Microwave Frequency Synthesizers

Alexander Chenakin

This tutorial provides a brief introduction to the field of frequency synthesis. It starts with general definitions and requirements followed by a review of the main synthesizer architectures. Direct analog, direct digital, and indirect techniques are compared in terms of performance, circuit complexity, and cost impact. The design tradeoffs are analyzed and complemented with a review of fractional-N, direct digital synthesizers (DDSs), frequency offset, multiloop, and other schemes. The current state and development trends of microwave frequency synthesizers will be reviewed.

Definitions and General Requirements

A frequency synthesizer is an electronic device that translates one (or more) input reference frequencies to a number of output frequencies, as illustrated in Figure 1. It can be treated as a "black box" containing individual components or building blocks, such as voltage-controlled oscillators (VCOs), frequency dividers, multipliers, mixers, phase detectors, etc., and when properly connected, it performs this translation function. Its structure is defined by a system architecture that describes the organization and relationships among the individual components [1].

An ideal synthesizer is intended to provide a pure sine-wave signal that, in the frequency domain, is represented as a pair of delta functions. Such an ideal signal would appear as a single tone (or, in other words, an indefinitely narrow line) on a spectrum analyzer screen. In reality, this line is spread by signal fluctuation effects (referred to as *phase noise* or *jitter*); some other signal artifacts (spurs and harmonics) are also present. In the time domain, these artifacts manifest themselves as signal waveform distortion. The quality and usability of the synthesized signal are determined by a few key parameters or specifications. The synthesizer's parameters can be divided into a few groups depicting its frequency and timing (frequency coverage, resolution, accuracy, and switching speed); spectral purity (harmonics,

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spurs, and phase noise); and other characteristics (output power, control range, step size, accuracy, impedance, and return loss).

Frequency and Timing

Frequency coverage or *range* denotes the range of frequencies that can be generated by the synthesizer. It is specified in the units of Hz (MHz and GHz) by indicating the minimum and maximum frequencies generated by the synthesizer.

Frequency resolution or *step size* is the maximum frequency difference between two successive output frequencies. The frequency coverage and resolution are fundamental synthesizer specifications set by a particular application. Some applications (e.g., test-and-measurement) require wide bandwidth and fine frequency resolution, while others need a relatively narrowband (10–20%) coverage with a rough step size or just a single fixed frequency.

Frequency accuracy indicates the maximum deviation between the synthesizer's set output frequency and its actual output. Frequency accuracy is normally determined by the reference signal, which can be internal or external to the synthesizer. Frequency synthesizers usually employ a crystal oscillator as an internal reference. The crystal oscillator's temperature stability and aging are important characteristics that define the synthesizer's frequency accuracy. *Temperature stability* denotes the maximum frequency drift over the operating temperature range and is usually expressed in ppm. The term *ppm* is an acronym for parts-per-million—a dimensionless coefficient equal to 10^{-6}. For example, the temperature stability of 0.5 ppm for a 100-MHz crystal oscillator means that the oscillator frequency can drift up to 50 Hz over the specified operating temperature range.

Aging is a change in frequency over time that occurs because of changes in the resonator material or a buildup of foreign material on the crystal. It is also specified in ppm over a certain period of time. Aging leads to a permanent frequency error; thus, it is good practice to use mechanical or electronic frequency adjustment means to compensate for internal reference aging. *Switching* or *tuning speed* determines how fast the synthesizer transitions from one desired frequency to another and is defined as time spent by the synthesizer between these two states (thus, *switching time* is a more proper term).

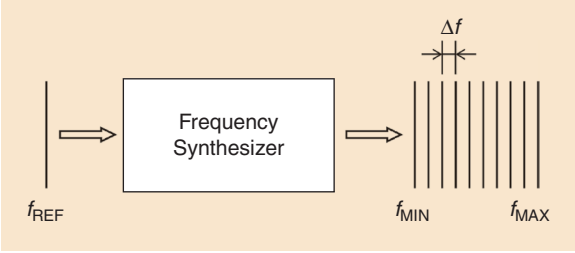

Figure 1. *Frequency synthesizer concept.*

Spectral Purity

Harmonics appear in the synthesizer spectrum as integer multiples of the output frequency because of signal distortion in nonlinear components. For example, if the fundamental frequency is represented by *f*, the frequencies of the harmonics would be represented by 2*f*, 3*f*, etc. Harmonics are expressed in dBc (decibels relative to the carrier) and represent the power ratio of a harmonic to a carrier signal. Harmonics usually do not cause serious problems since they are well separated from the main tone and can be easily filtered out. Moreover, they are often recreated in a nonlinear device (such as a mixer) connected to the synthesizer. The range of –15 to –30 dBc is acceptable in many cases, although the level should be reduced to –60 dBc or even lower in some harmonic-sensitive applications, such as test-and-measurement instruments. For a narrowband synthesizer, this is easily achieved by placing a low-pass filter (LPF) at the output. A switched filter bank or a tunable filter is required for bandwidths reaching or exceeding an octave.

Subharmonics are created at frequencies that are "subharmonically" related to the main signal, such as *f*/2, *f*/3, etc. A typical example that can demonstrate the creation of subharmonics is a frequency doubler, which is often used to extend the synthesizer output frequency range. As a nonlinear device, the doubler generates a number of harmonics of the incoming signal. Since the second harmonic now becomes the main signal, all the odd products do not meet the harmonic relationship with respect to the desired output and are, therefore, treated as subharmonics. Similar to harmonics, the subharmonics of a small order (e.g., one-half or one-third) are well separated from the main output, and, hence, can be easily filtered. However, high-order products can present a serious problem due to decreasing separation from the main tone. As a common rule, the subharmonics are normally treated as spurious (i.e., nonharmonically related) signals.

*Spurious signal*s or *spurs* are undesired artifacts created by the synthesizer at some discrete frequencies that are not harmonically related to the output signal. Spurs can come from different sources, such as phase-locked loop (PLL) reference spurs, mixer intermodulation products and local oscillator (LO) leakage, some internal auxiliary signals, or even external signals

coming through the bias or control interface. Although the spurs seem randomly positioned in the synthesizer spectrum, their location is mostly determined by a particular synthesizer architecture and frequency plan. In contrast to harmonics, the spurs are much more troublesome products that can limit the ability of receiving systems to resolve and process a desired signal. Spurs can sit very close to the main tone and in many cases cannot be filtered. Thus, the spurious level has to be minimized, typically to –60 dBc relative to the main signal, although many applications require bringing this level even lower. This presents a certain design challenge, especially if a small step size is required. A different concern is mechanically induced spurs, usually referred to as *microphonics*. These spurs appear due to the sensitivity of certain synthesizer components to external mechanical perturbations and are treated by mechanical (e.g., damping) and electrical (e.g., wideband PLL) means.

Phase noise is a measure of the synthesizer's short-term frequency instability, which manifests itself as random frequency fluctuations around the desired tone. Phase noise is one of the major parameters that ultimately limits the performance of RF and microwave systems. To illustrate this, let's examine the ability of a microwave receiver to resolve a signal of small amplitude. The receiver is essentially a mixer that converts the signal down and processes it at a lower intermediate frequency (IF). Naturally, the conversion is affected by the quality of the available LO source, as illustrated in Figure 2. A receiver utilizing an LO source with excessive phase noise (source A) will not be able to detect the signal since it is masked under the phase noise. To receive the desired signal, either the transmitter has to provide higher output power, or a better LO source (source B) is required. Therefore, phase noise generated by the frequency synthesizer is a critical parameter that imposes the ultimate limit on the system's ability to resolve signals of small amplitude. Phase noise minimization is a primary design concern—it demands a specific effort and usually results in a tradeoff between other synthesizer parameters.

Other Parameters

Output power is a measure of the synthesizer output signal strength specified in units of watts or, more frequently, in dBm. The term *dBm* refers to the ratio in decibels of the measured power referenced to 1 mW. The RF output power can vary within a wide range depending on a particular application. A typical scenario assumes the frequency synthesizer as an LO source driving a frequency mixer in a variety of up- and downconversion schemes. This normally requires a 10–17-dBm output signal, although some applications need more power. A simple synthesizer usually

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delivers a fixed power level that cannot be changed. More complex designs provide an ability to control the output power in a specified range. In the latter case, the output power control range (i.e., the minimum and maximum values between which power can be set) and the power step size (i.e., the minimum change between two consecutive power settings) are specified as well. Note that output power can differ from its set value. This discrepancy is described by the output power accuracy, which defines the absolute maximum variance between programmed and actual (i.e., measured) power values.

Output impedance is an important characteristic since RF and microwave devices are supposed to be matched with other devices when connected. At microwave frequencies, the source and load impedances are normally set to 50 Ω, although some equipment works in other environments, e.g., 75 or 600 Ω. When the source and load impedances are mismatched, some incident power is reflected back. As a result, not all of the available power from the source is delivered to the load. The return loss (measured in dB) is used to quantify such a mismatch; it indicates how close the synthesizer output impedance is to 50 Ω (or another specified value). The best scenario assumes no reflection, which corresponds to a negligibly small return loss. On the other hand, a return loss of 0 dB corresponds to total reflection when all incident power is reflected. Alternatively, the output match can be described by the voltage standing wave ratio (VSWR). A VSWR of 2:1 (which roughly corresponds to a –10-dB return loss) is typically an acceptable level for many synthesizer designs.

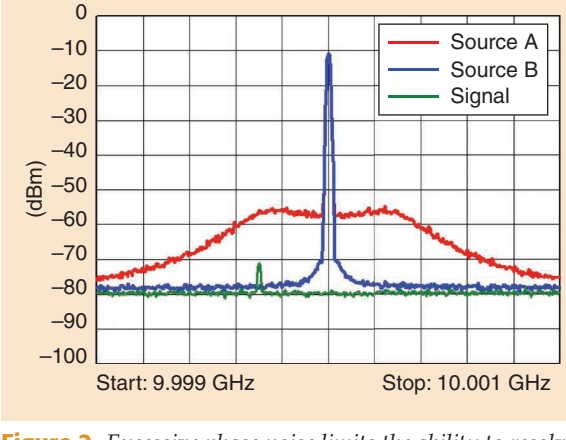

Figure 2. *Excessive phase noise limits the ability to resolve a signal of small amplitude.*

Direct analog synthesis is one of the most powerful techniques, offering excellent switching speed and phase noise performance.

A better match is required for some demanding applications and can be achieved by connecting an attenuator to the synthesizer output.

Other specifications may include power supply (dc or ac voltage, current, and power consumption) and mechanical (size, weight, and mounting dimensions) and environmental (temperature, humidity, altitude, and vibration) characteristics as well as some special features, such as dual output (or a number of outputs), various modulation options, and many other functions tailored to specific applications.

Architectures

Synthesizers come in a variety of forms, ranging from tiny PLL chips and moderate-size modules to benchtop signal generators. The RF/microwave industry is under persistent pressure to deliver higher performance, higher functionality, smaller size, lower power consumption, and lower cost synthesizer designs [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22]. Although all synthesizers exhibit significant differences as a result of specific applications, they share basic fundamental design objectives. The ideal synthesizer should preferably be broadband with fine frequency resolution, which allows for addressing a larger number of potential applications. Aside from frequency coverage and resolution, phase noise and spurs are critical parameters that impose the ultimate limit on the system's ability to resolve signals of small amplitude.

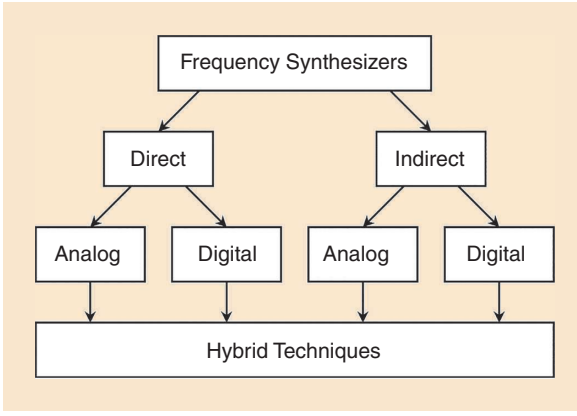

Figure 3. *Frequency synthesizer architecture.*

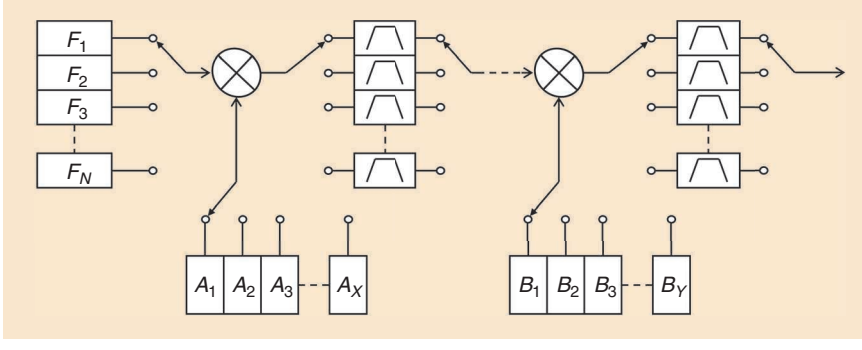

Figure 4. *Direct analog synthesizer.*

Another key parameter of the synthesizer that impacts overall system performance is the frequency switching speed. The time spent by the synthesizer transitioning between frequencies becomes increasingly valuable since it cannot be used for data processing. Modern synthesizers tend to be faster due to the ongoing increase of the data rates of RF/microwave systems. Another challenge is size and cost reduction. These requirements—wide frequency coverage, small step size, fast switching speed, low phase noise, and spurious—are the key drivers in the development of modern frequency synthesizers.

Synthesizer characteristics depend heavily on a particular architecture that is usually classified into direct and indirect groups, as illustrated in Figure 3. The direct architectures are intended to create the output signal directly from the available reference signals either by manipulating and combining them in the frequency domain (direct analog synthesis) or by constructing the output waveform in the time domain (direct digital synthesis). The indirect methods assume that the output signal is regenerated inside the synthesizer in such a manner that the output frequency relates (e.g., is phase locked) to the input reference signal. A practical synthesizer, however, is usually a hybrid design that combines various techniques to take advantage of the best aspects of each.

Direct Analog Synthesizers

Direct analog synthesis is one of the most powerful techniques, offering excellent switching speed and phase noise performance [18], [19]. As the name suggests, the desired signal is created directly (i.e., without regeneration) by mixing base frequencies followed by switched filters, as conceptually shown in Figure 4. The base frequencies can be obtained by frequency multiplication, division, and/or mixing.

The key advantage of the direct analog technique is extremely fast switching speed, ranging from microseconds to nanoseconds. Since direct

analog synthesis assumes no closed loops, switching speed is limited only by propagation delays inserted by the switches and their control circuits as well as filter settling. Another distinct advantage is the ability to generate low phase noise due to the usage of components with negligibly low residual noise compared to the base frequency sources. Hence, the direct analog synthesizer phase noise mainly depends on the noise of the available fixed-frequency sources and can potentially be very low. The main disadvantage of the indicated topology is limited frequency coverage and step size. The number of output frequencies can be further increased by using a higher number of base frequencies and/or mixer stages. However, this rapidly increases the design complexity and overall component count.

A serious problem associated with direct analog synthesis is the large number of mixing products that have to be filtered. These include the undesired mixer sideband, LO leakage, and intermodulation products. Depending on a particular frequency plan, filtering close-in spurs can be a challenging task.

Another promising approach is based on the concept of the consecutive spreading of the synthesizer's operating frequency bandwidth [27]. Such a synthesizer structure consists of several cascades that include a programmable frequency divider, mixer, and bandpass filter (or switched filter bank). Several frequencies generated by the programmable divider are mixed with the input LO signal, as illustrated in Figure 5. The input frequency bandwidth and division coefficients are selected in such a manner that $\Delta f_{i+1} > \Delta f_i$ with continuous coverage. Therefore, every mixer stage increases the operating bandwidth until it reaches a desired value, as depicted in Figure 6.

Although a large variety of mixing and filtering schemes are possible, they tend to be hardware intensive if a small frequency step and wide coverage are required. Therefore, while direct analog synthesis offers excellent tuning speed and phase noise characteristics, its usage is limited to applications where a fairly high cost can be tolerated. This includes radars, frequency hopping and antijam communications, high-throughput ATE, medical imaging systems, and other applications that demand speed.

DDSs

In contrast to traditional analog concepts, DDSs utilize digital signal processing to construct an output signal waveform in the time domain piece by piece from a reference clock signal [16]. A general DDS block diagram consists of four main blocks: a phase accumulator, digital lookup table (LUT), digital-to-analog converter (DAC), and LPF, as depicted in Figure 7.

The heart of a DDS is a phase accumulator (Figure 8) that allows entering a digital word called the *phase increment*. At each clock pulse, the phase accumulator adds (accumulates) the increment to the previously stored digital value that represents an instantaneous digital phase of the generated signal. This digital phase is updated until it reaches the capacity of the accumulator. For an N-bit accumulator and the smallest increment of one least significant bit, it will take 2^N clock cycles to fill up the accumulator. Then, the accumulator resets, and the process starts over again. Hence, the lowest generated frequency is given by

$$f_{\text{MIN}} = \frac{f_{\text{CLK}}}{2^N}$$

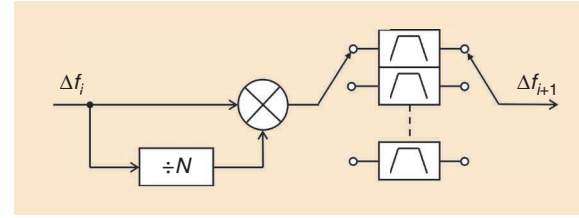

Figure 5. *Frequency bandwidth spreading.*

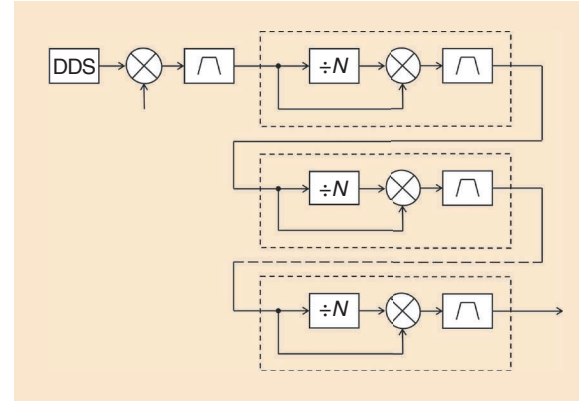

Figure 6. *Using consecutive spreading in direct analog synthesis.*

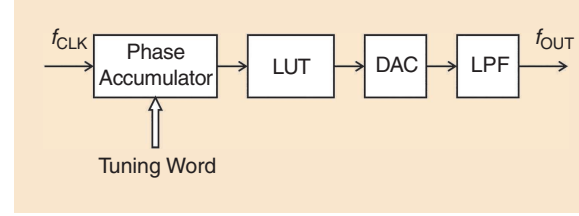

Figure 7. *A DDS. LUT: lookup table; DAC: digital-to-analog converter; CLK: clock.*

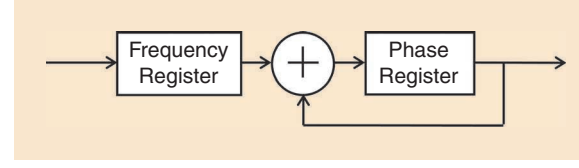

Figure 8. *Phase accumulator.*

The most valuable DDS feature is its exceptionally fine frequency resolution; sub-Hz levels are easily achieved.

which also equals the smallest frequency step. With a larger phase increment (W), the phase accumulator fills up faster, and the DDS output frequency increases to

$$f_{DDS} = \frac{W}{2^N} f_{CLK}.$$

Therefore, frequency tuning is accomplished by changing the phase increment word. This process is extremely fast and is mainly limited by the digital control interface. This results in very high switching speeds that are comparable with direct analog schemes. DDS also provides reasonably low phase noise, even showing an improvement (limited by its residual noise floor) over the phase noise of the clock source itself. However, the most valuable DDS feature is its exceptionally fine frequency resolution; sub-Hz levels are easily achieved. The main disadvantage is limited usable bandwidth. While DDS starts working from nearly dc, its highest frequency is limited by the Nyquist criteria within one-half of the clock frequency. Working in higher Nyquist zones is possible; however, the performance degrades very fast. Another serious problem is a relatively high spurious content due to a number of factors inherent in the DDS technique, such as bit truncation, quantization, DAC conversion errors, etc.

DDS are available as specialized fully integrated ICs, or they can be built using separate field-programmable gate arrays (FPGAs) and DAC ICs. The latter allows constraining the digital part within the FPGA, thus isolating its electromagnetic interference-induced spurs. Today's FPGAs have the sufficient capacity to build quite complex multicore phase accumulators and LUT with negligible spur levels due to bit truncation. As a result, the major spur sources are normally on the DAC side due to their nonlinearities and quantization noise. Wider frequency coverage is possible using two or more DACs in an interleaved data mode. DAC-free solutions are also possible, for example, using digital-to-time conversion [26], although they are not so common.

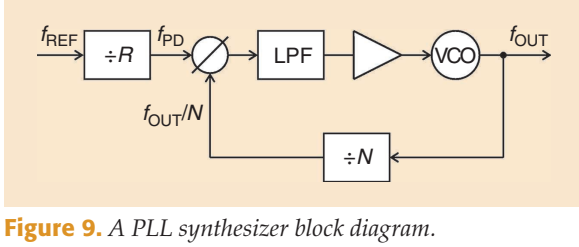

Figure 9. *A PLL synthesizer block diagram.*

Until recently, the DDS technique was rarely used alone at microwave frequencies. However, the rapid development of high-frequency ICs enables DDS to work directly at microwave frequencies with quite impressive characteristics, such as microhertz resolution, nanosecond-range switching speed, and built-in modulation. The extension of usable DDS bandwidth (together with its spur content reduction) is the key improvement required by the industry.

Indirect Synthesizers

Indirect frequency synthesizers are commonly associated with PLL techniques that utilize a high-frequency oscillator to generate an output signal that is in a certain relationship with the reference signal [8], [9], [10]. A typical single-loop PLL synthesizer includes a tunable VCO that generates a signal in a desired frequency range, as illustrated in Figure 9. This signal is fed back to a phase detector through a frequency divider with a variable frequency division ratio N. The other input of the phase detector is a reference signal equal to a desirable step size. The phase detector compares the signals at both inputs and generates an error voltage that, following filtering and optional amplification, slews the VCO until it acquires the lock frequency given by

$$f_{OUT} = N f_{PD}$$

where f_{PD} is the comparison frequency at the phase detector inputs. The frequency tuning is achieved in discrete frequency steps equal to f_{PD} by changing the division coefficient N. The available reference frequency can be divided down by another divider to reduce the step size if needed.

The major advantages of the PLL scheme are reduced levels of spurious signals resulting from the LPF action of the loop and the much lower level of complexity compared to the direct analog architectures. The loop filter bandwidth has to be significantly lower than f_{PD} (usually 10 times or more) to keep the reference spurs at a reasonable level. However, the loop bandwidth is inversely proportional to the settling time. Thus, achieving fine frequency resolution, low spurs, and fast switching is an arduous task as it means balancing mutually exclusive terms. Another important consideration and design tradeoff is phase noise. The noise outside of the PLL filter bandwidth is mainly determined by the VCO's free-running noise. The phase noise within the loop filter bandwidth is given by

$$\mathscr{L}_{PLL} = \mathscr{L}_{\Sigma PD} + 20 \log N$$

where $\mathscr{L}_{\Sigma PD}$ is the cumulative phase noise of the reference signal, reference and feedback dividers, phase detector, LPF, and loop amplifier recalculated to the

phase detector input, as illustrated in Figure 10. In other words, the phase noise generated by PLL components is degraded by large division ratios required to provide a high-frequency output with a fine resolution. For example, to get 10-GHz output with a 1-MHz step size, the feedback divider ratio has to be 10,000, which corresponds to 80 dB of phase noise degradation! Thus, the conventional single-loop architecture suffers from mutually exclusive design goals. It is usually utilized in nondemanding applications or when low cost is the major concern.

Fractional-N synthesizers break this coupling between frequency resolution and other characteristics by using fractional division ratios and, therefore, allowing a higher comparison frequency for a given step size. For example, if we need to generate some frequencies around 10 GHz with a 1-MHz step size (i.e., 10.000, 10.001, 10.002 GHz, etc.), the phase detector comparison frequency should equal 1 MHz, and the division coefficients should be set to 10,000, 10,001, 10,002, etc. Note that we could get these frequencies using a 10-MHz reference if we could set the loop division coefficient to fractional numbers, i.e., 1,000 + 0/10, 1,000 + 1/10, 1,000 + 2/10, etc. Thus, we would be able to reduce the maximum loop division ratio by about 10 times and use a significantly higher phase detector comparison frequency that would benefit virtually all synthesizer parameters.

Fractional ratios are possible by alternating two (or more) division ratios (let's say, N and $N + 1$) and averaging the output frequency over a certain period of time. Another way to look at this process is to calculate the number of pulses delivered by such a complex divider for a given time interval. Obviously, the average division coefficient will be between N and $N + 1$ depending on how many pulses are processed by each individual divider. The biggest concern associated with this scheme is that the instant frequency at the fractional-N divider output is not constant. An abrupt change in the division coefficient leads to a phase discontinuity that produces a voltage spike at the phase detector output. Since the frequency division change occurs periodically with the same rate, it appears as discrete spurs in the synthesizer's output spectrum. Suppression of the resulting spurs requires the PLL filter bandwidth to be sufficiently small, which may affect the phase noise and speed performance.

There are many techniques to reduce fractional-N spurs [23], [24], [25]. In general, this can be accomplished by adding or subtracting a voltage at the phase detector output during the frequency division change. Another method is based on using a multimodulus divider that allows a larger number of division coefficients. In this case, one should expect a larger number of spurs of smaller amplitude. The multimodulus divider is often accompanied by a delta-sigma modulator that allows randomizing frequency spurs and pushing them toward higher offset frequencies where they can be filtered by the loop filter. In spite of various improvements, the main disadvantage of the fractional-N technique is the excessive spurious levels produced by phase errors inherent in the fractional division mechanism.

A clever method to reduce fractional spurs is to utilize a variable reference. The technique is based on the fact that spur location in a fractional-N synthesizer is a function of its particular division ratio and output frequency. Therefore, for a given output frequency, one can move (and then filter out) an undesired spur by changing the reference frequency and corresponding division ratio. This involves thorough frequency planning and also requires an additional frequency synthesizer (to be used as a reference). Furthermore, although the division ratio is reduced, it can still be high enough to affect PLL performance.

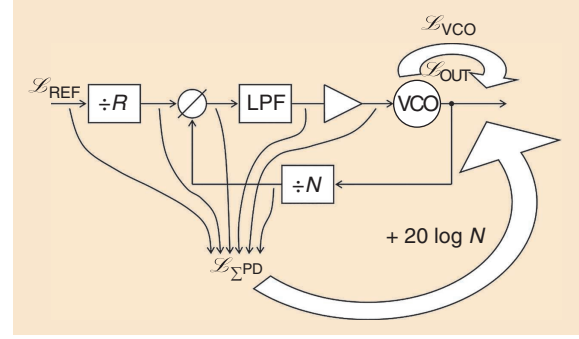

Figure 10. *PLL noise sources.*

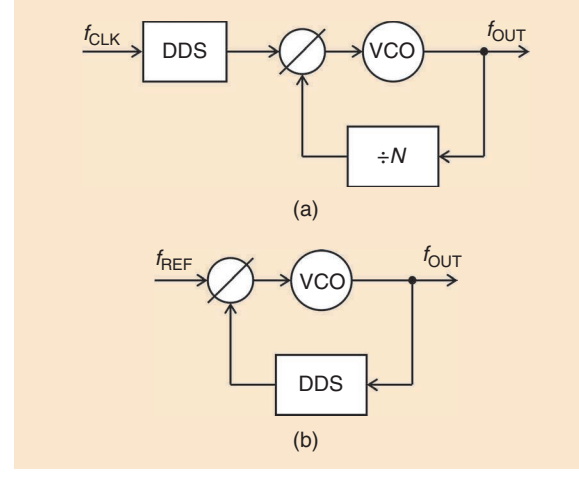

Figure 11. *(a) and (b) Using a DDS within a PLL synthesizer.*

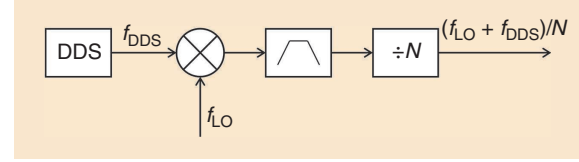

Figure 12. *Upconverting and dividing DDS signal.*

The DDS is another effective solution to provide a very fine frequency resolution without a common penalty of the phase detector comparison frequency reduction. The DDS can serve as a fine-resolution high-frequency reference or be employed as a fractional divider, as shown in Figure 11. While a DDS provides excellent frequency resolution, its spurious levels are usually quite high. Moreover, the spurs further degrade because of the PLL multiplication mechanism. Although the two schemes in Figure 11 look different, they both affect DDS spurs in the same manner. In both cases, the overall loop division coefficient is defined by the ratio between the VCO output and phase detector comparison frequencies.

The DDS spurs can be reduced utilizing many techniques, for example, using a variable clock (as described previously for the fractional-N synthesizers) or upconverting and further dividing down the DDS signal, as illustrated in Figure 12. Note that the upconverted relative DDS bandwidth is reduced and often needs further extending as required by a particular frequency plan. This can be achieved by various methods, for example, using not fixed by variable frequency division coefficients.

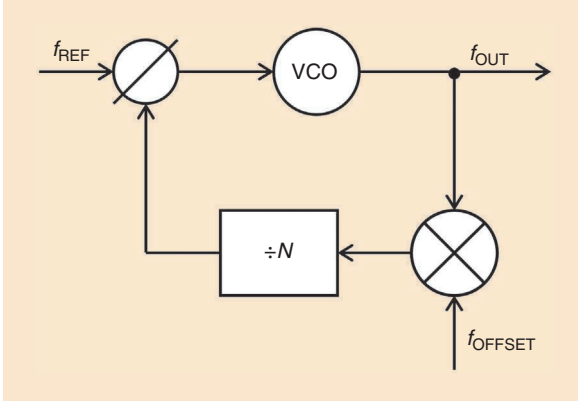

Figure 13. *Frequency mixing within PLL feedback path.*

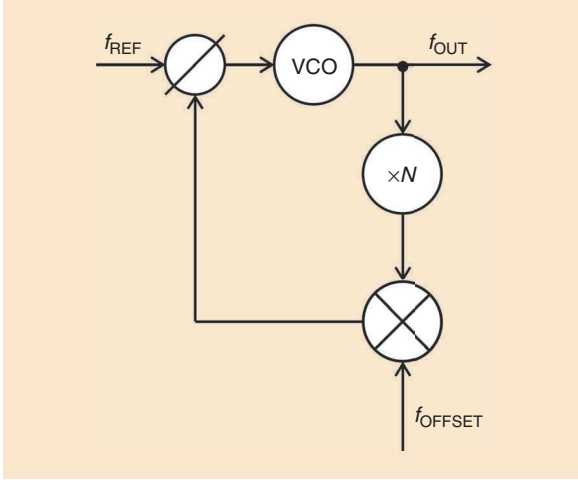

Figure 14. *A frequency multiplier in the feedback path improves PLL noise performance.*

The synthesizer's main characteristics can be drastically improved using frequency conversion (mixing) within the synthesizer feedback path, as shown in Figure 13. The idea is to convert the VCO output to a much lower frequency with the aid of a mixer and an offset frequency source. In certain scenarios (e.g., when the operating frequency range is narrow), it is possible to eliminate the feedback frequency divider completely. In this case, the loop division coefficient equals one, and no phase noise degradation occurs. Moreover, one can further reduce the PLL components' residual noise by inserting a frequency multiplier into the feedback path instead of a divider, as depicted in Figure 14.

Therefore, there can be three basic scenarios for constructing a PLL, as follows:

$N > 1$: a frequency divider within the PLL loop (residual phase noise is degraded at $20\log N$)

$N = 1$: no division within the PLL loop (residual phase noise is not degraded)

$N < 1$: a frequency multiplier within the PLL loop (residual phase noise is improved at $20\log N$).

The main disadvantage of simple frequency offset schemes is the limited frequency coverage. Widening

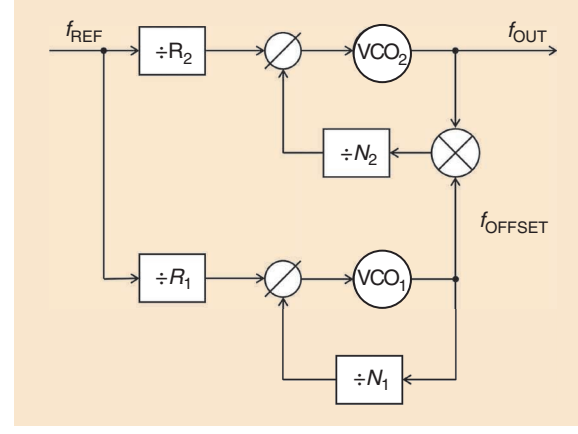

Figure 15. *Multiloop synthesizer.*

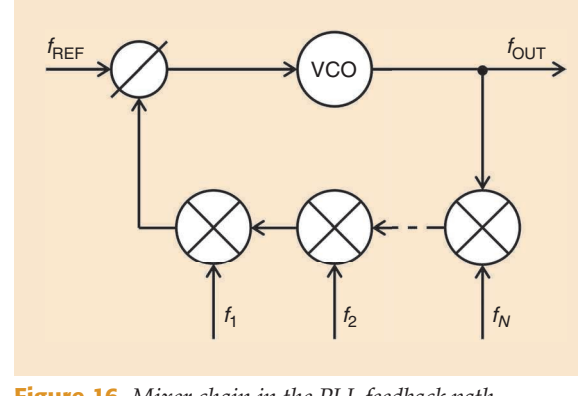

Figure 16. *Mixer chain in the PLL feedback path.*

the output frequency bandwidth for a fixed offset frequency leads to a higher IF at the mixer output. This requires a divider with a larger division coefficient, thus defeating the idea of this method. The offset frequency signal should preferably be as close as possible to the RF output frequency to keep the division ratio at a minimum. This can be accomplished in multiloop schemes by utilizing a wideband offset signal (Figure 15).

Another solution is to utilize a chain of mixers within the PLL feedback path, as illustrated in Figure 16. Individual offset signals and phase detector references can be obtained from a common high-frequency variable reference using dividers, as depicted in Figure 17.

One of the problems associated with any frequency-mixing scheme is a possible false lock caused by undesired mixing products. The easiest solution to prevent a false lock is to restrict the VCO from going outside an acceptable frequency range. For a narrowband synthesizer, this can be accomplished by selecting a VCO with a sufficiently narrow tuning range and/or properly limiting its tuning voltage. Another method, also applicable for wideband applications, is to pretune a VCO to approximately the correct frequency where it can be caught by the PLL circuit. This can be achieved with a DAC, as depicted in Figure 18. The VCO tuning port is initially connected to the DAC that generates a required voltage for coarse tuning. Then, the VCO switches to the PLL and eventually locks to the exact frequency. Although it seems very straightforward, this acquisition aid requires linear and repeatable VCO tuning characteristics as well as precise frequency calibration to compensate for the VCO temperature drift.

A VCO can also be pretuned with an auxiliary coarse-tuning PLL circuit that does not utilize frequency mixing, and hence, avoids output frequency uncertainty. Inserting an additional divider (which bypasses the mixer, as depicted in Figure 19) forms the coarse-tuning PLL. The output of this divider connects to the phase detector with a switch. Initially, the switch is in the upper position, thus engaging the coarse-tuning PLL. The coarse-tuning PLL is a conventional single-loop circuit that provides a simple and reliable mechanism to pretune the VCO to a desired frequency. It also generates a lock detect signal indicating that the frequency acquisition is completed. Then, the switch disconnects the coarse-tuning path and connects the offset mixer chain. The synthesizer relocks to the desired frequency, providing better spectral purity performance. The phase noise and spurious characteristics of the coarse-tuning PLL are not a big concern since this path is completely disabled after the initial frequency acquisition. The main advantage of this method is that the coarse-tuning mechanism does not depend on the VCO temperature drift or any other component instabilities. The frequency acquisition accuracy is entirely a function of the auxiliary loop characteristics (step size) and can be easily improved using a DDS or a fractional-N scheme.

The practical implementation of this method may face some difficulties since the loop gain changes significantly when the circuit switches the PLL paths. Furthermore, the phase detector comparison frequency may also need changing. Another way to implement the coarse-tuning PLL concept is presented in Figure 20. The scheme includes two separate phase detectors and reference dividers; therefore, both PLLs can be designed and optimized independently.

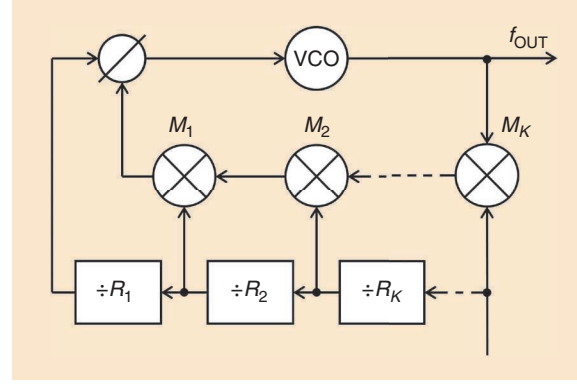

Figure 17. *Creating LO signals from a common reference.*

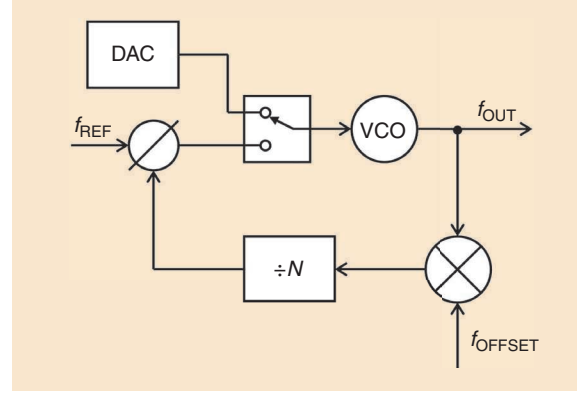

Figure 18. *Initial frequency acquisition using a DAC.*

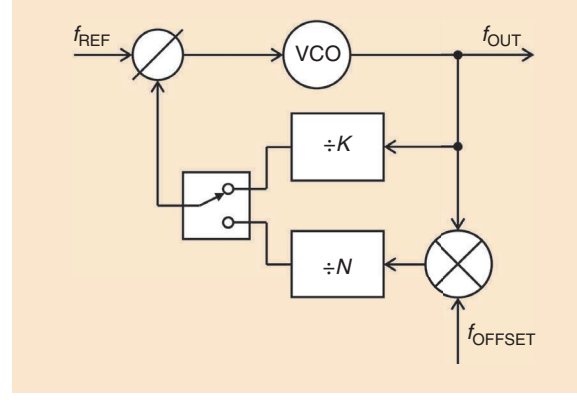

Figure 19. *Pretuning with an additional PLL circuit.*

Figure 21 presents a more general block diagram combining the advantages of the previously described circuits. The presented solution is capable of generating a high-frequency signal with a low phase noise, low spurious level, and fast switching speed [28]. In this block diagram, a VCO output signal is converted in mixers M_1-M_i to the phase detector comparison frequency F_0 equal to the synthesizer step size. The comparison frequency, as well as mixer LO signals, is produced from a common high-stable low phase noise reference signal using frequency dividers with frequency division ratios D_1-D_i and frequency multipliers with multiplication factors C_1-C_i, respectively. A phase detector compares the signals at both inputs and generates an error voltage that slews the frequency of the VCO to a lock frequency given by

$$f = f_i \pm f_{i-1} \pm \cdots \pm f_2 \pm f_1 \pm F_0$$

or after simple manipulations

$$f = F_0(D_1D_2\ldots D_{i-1}D_iC_i \pm D_1D_2\ldots D_{i-1}C_{i-1} \pm \cdots \pm D_1D_2C_2 \pm D_1C_1 \pm 1).$$

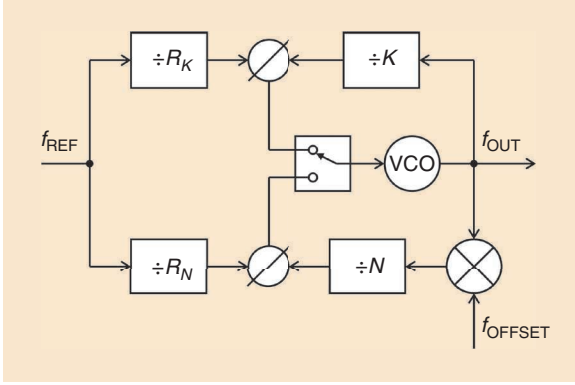

Figure 20. *Two phase detectors simplify circuit design.*

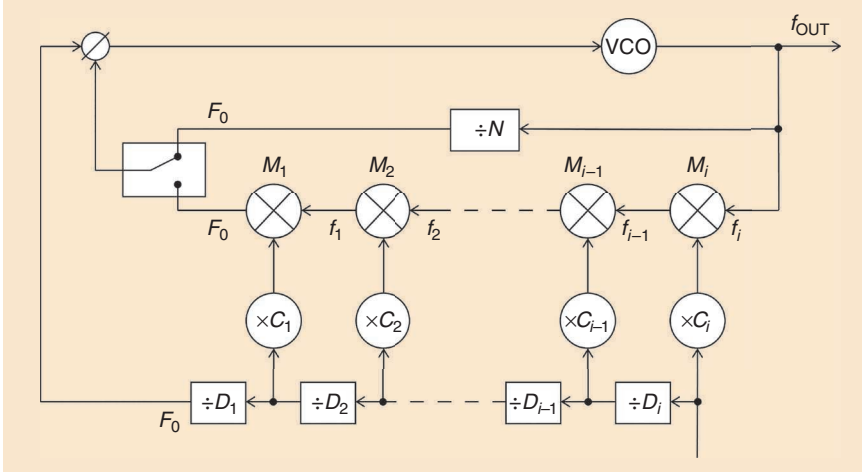

Figure 21. *Using frequency coarse tuning and multiple mixers within the PLL loop.*

Since all the division and multiplication coefficients are integer numbers, we can write

$$f = F_0 \times N$$

where $N = (D_1D_2\ldots D_{i-1}D_iC_i \pm D_1D_2\ldots D_{i-1}C_{i-1} \pm \cdots \pm D_1D_2C_2 \pm D_1C_1 \pm 1)$ is an integer.

A desired output frequency can be chosen using an additional coarse-tuning divider with a programmable division ratio N inserted into the synthesizer loop. The divider provides a simple and reliable mechanism to pretune the VCO to exactly the correct frequency. Then, the switch turns off the divider feedback path and connects the mixer chain to ensure that no phase noise degradation occurs. An important feature of this method is also that the mixers do not generate undesired products within the synthesizer loop bandwidth. The output of every mixer includes a vast number of products, including the fundamentals of the mixer's RF and LO signals and their harmonics, and the sums and differences of the RF and LO and their harmonics given by

$$f_{MIX} = \pm mf_{RF} \pm nf_{LO}$$

which can be written for the mixer M_i as

$$f_{MIXi} = \pm mF_0N \pm nF_0D_1D_2\ldots D_{i-1}D_iC_i.$$

Assuming that all the coefficients are integers, the mixer products are given by

$$f_{MIXi} = kF_0$$

where k is an integer number. Similarly, it can be shown that all harmonic and intermodulation products generated by the mixer chain are multiples of the phase detector frequency F_0, which can be easily rejected by a PLL loop filter.

This method was successfully implemented in the QuickSyn® frequency synthesizer module (presented by Phase Matrix, Inc. in 2008) capable of generating a very clean signal with wideband frequency coverage and fine resolution. Specifically, this synthesizer demonstrated –122-dBc/Hz phase noise at 10-GHz output and 10-kHz offset along with 100-uS switching speed [29].

Generation of Reference Frequency

Phase noise of modern microwave synthesizers mainly depends on

references such as 100-MHz oven-controlled crystal oscillators (OCXOs). The 100-MHz OCXO can be locked to a 10-MHz OCXO to reduce phase noise at low-frequency offsets. Similarly, a higher frequency oscillator (such as the surface acoustic wave of DRO) can be added to improve phase noise at higher frequency offsets. A combined reference source (which contains several oscillators locked to each other) can be used to achieve the lowest phase noise profile at any frequency offset. This approach was successfully used in the Rubidium™ signal generators (Figure 22) presented by Anritsu Company in 2021 [6]. The synthesizer core is based on a proprietary 2–20-GHz YIG oscillator that is locked to an internal reference extracted and distributed by direct analog means, as illustrated in Figure 23.

Figure 22. *A Rubidium™ signal generator.*

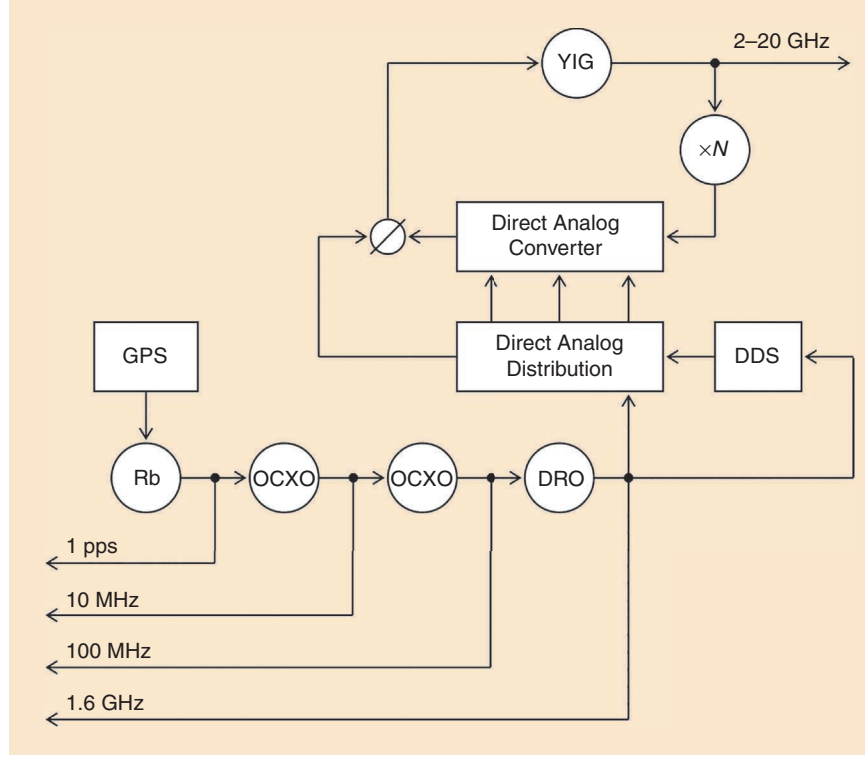

Figure 23. *A simplified block diagram of the Rubidium™ synthesizer core.*

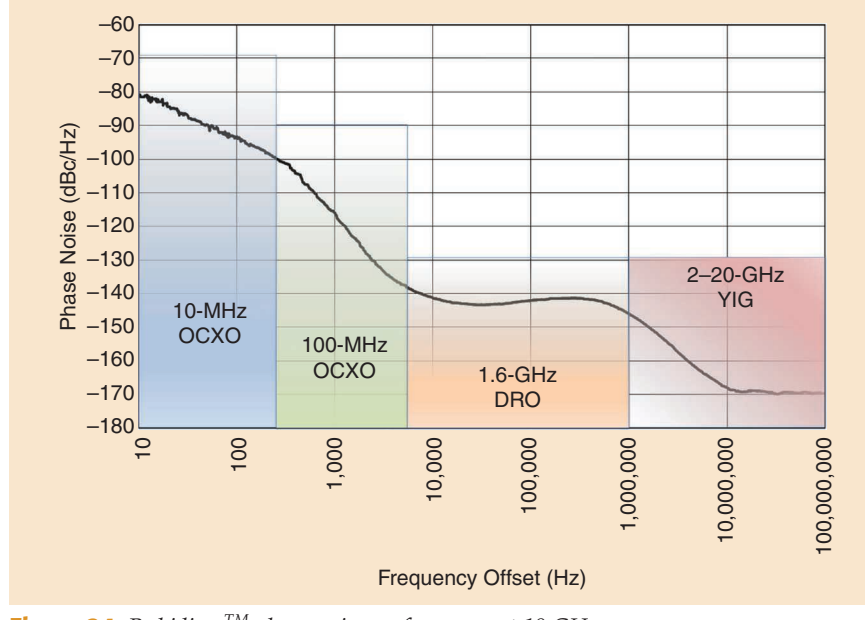

Figure 24. *Rubidium™ phase noise performance at 10 GHz.*

The YIG native frequency coverage is further extended with a frequency multiplier and frequency divider (followed by a high-power amplifier, amplitude control, and harmonic filtering) to achieve 9 kHz to 20 GHz or 43.5-GHz coverage. The YIG output signal is downconverted by a direct analog converter (which is essentially a chain of mixers) that eliminates any frequency divider and, therefore, phase noise degradation within the PLL. Furthermore, a switched frequency multiplier is inserted into the loop that provides additional residual PLL noise suppression. As a result, the presented architecture provides an essentially noiseless PLL mechanism, meaning that it translates the synthesizer's reference noise with minimal added phase noise degradation.

A three-source combined reference is utilized to provide the lowest possible phase noise at any given frequency offset. Furthermore, the combined reference is disciplined by a rubidium atomic clock that introduces a much higher

Overall, the RF/microwave industry is under persistent pressure to deliver higher performance synthesizer designs.

degree of stability compared to a conventional OCXO-based reference. The rubidium clock operation is based on fundamental constants rather than physical dimensions and, hence, is extremely stable. This architecture delivers fairly high performance with respect to spectral purity and stability. Phase noise of –140 dBc/Hz at 10-GHz and 10-kHz output was measured, as shown in Figure 24.

Conclusion

Overall, the RF/microwave industry is under persistent pressure to deliver higher performance synthesizer designs. Demand is driven by the wireless communications, aerospace and defense, and automotive industries as well as new technologies such as 6G [30]. As of today, traditional indirect PLL architectures still dominate. On the other hand, direct analog synthesis is the most advanced approach that demonstrates extremely fast switching speed and low phase noise. Although direct analog synthesizers are usually quite expensive, nevertheless, they can be successfully used in some applications where a fairly high cost can be tolerated. However, future developments are associated with direct digital synthesis due to the rapid progress in solid-state technologies. The extension of DDS usable bandwidth to several tens of gigahertz with its spurious content reduction is expected. Further major breakthroughs are expected operating the reference with other physical principles or materials such as sapphire-loaded cavity oscillators with combined frequency stabilization as well as optoelectronic methods [31], [32], [33], [34].

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