# Synthesizers: Looking Beyond the Basics

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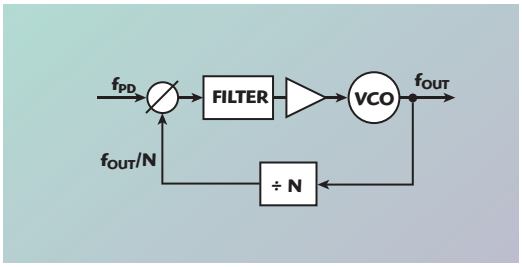
*Fractional-N PLL synthesizers are among the most challenging of high-frequency designs. Many approaches have been developed to generate clean output signals, although techniques that achieve fine frequency resolutions often suffer from elevated spurs and phase noise. In this article, industry expert Dr. Alexander Chenakin reveals the anatomy of the fractional-N synthesis and discusses some new ways to go beyond the current technology limits.*

A generic single-loop PLL synthesizer includes a tunable VCO that generates a signal in a desired frequency range. This signal is fed back to a phase detector through a frequency divider with a variable frequency division ratio N as depicted in ***Figure 1***. The other input of the phase detector is a reference signal equal to a desirable step size. The phase detector compares the signals at both inputs and generates an error voltage, which following filtering (and optional amplification) slews the VCO until it acquires the lock frequency given by $f_{OUT} = N f_{PD}$, where $f_{PD}$ is the comparison frequency at the phase detector inputs. Thus, the frequency tuning is achieved in discrete frequency steps equal to $f_{PD}$ by changing the division coefficient N.

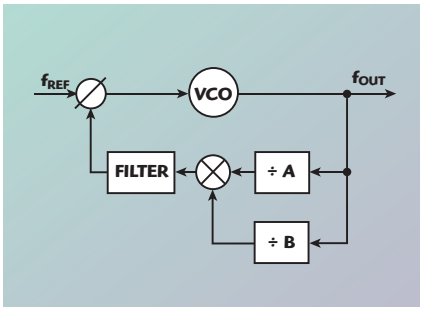



▲ *Fig. 1 Single-loop PLL synthesizer.*

This simple PLL synthesizer exhibits various limitations and tradeoffs. The main impact on the synthesizer performance is due to large division ratios required to provide a high-frequency output with a fine resolution. Note that any noise generated by PLL components is degraded at 20logN rate, where N is the division ratio. In conventional integer-N PLLs operating at small step sizes, the division ratio is large because the step size must be equal to the comparison frequency at the phase detector. As a result, significant phase noise degradation occurs. Furthermore, the synthesizer switching speed is a function of its loop bandwidth and, therefore, is limited by the phase detector comparison frequency too.

## CONVENTIONAL DESIGNS

Fractional-N synthesizers break this coupling between frequency resolution and other




▲ *Fig. 2 Self-offset scheme.*

characteristics by using fractional division ratios and, therefore, allow a higher comparison frequency for a given step size. How are fractional division coefficients realized? In general, it is possible by alternating two division ratios (let's say, N and N+1) and averaging the output frequency over a certain period of time. Another way to look at this process is to calculate the number of pulses delivered by such a divider for a given time interval. Obviously, the average division coefficient will be between N and N+1 depending on how many pulses are processed by each divider.

The biggest concern associated with this scheme is that the instant frequency at the fractional-N divider output is not constant. An abrupt change in the division coefficient leads to a phase discontinuity that produces a voltage spike at the phase detector output. Since the frequency division change occurs periodically with the same rate, it appears as discrete spurs in the synthesizer's output spectrum. Suppression of the resulting spurs requires that the PLL filter bandwidth has to be sufficiently small, which is not always possible.

There are many techniques to reduce fractional-N spurs.[1-11] In general, this can be accomplished by adding or subtracting a voltage at the phase detector output during the frequency division change. Another method is based on using a multi-modulus divider that allows a larger number of division coefficients. In this case, we should expect a larger number of spurs of smaller amplitude. The multi-modulus divider is often accompanied by a delta-sigma modulator. The delta-sigma technique is well known in communication systems and has been used extensively for analog-to-digital conversion. The fundamental idea of utilizing ΔΣ-modulators is to shape the quantization noise in such a way that a smaller amount of noise power remains within the utilized signal bandwidth.

The same idea can be successfully applied to fractional-N frequency synthesis applications by randomizing frequency spurs and pushing them towards higher offset frequencies where they can be easily filtered by the loop filter. Moreover, a ΔΣ-modulator can also reshape the residual noise spectrum so that it has more power at higher frequency offsets. Accompanied by a properly designed loop filter, this leads to better spurious and phase noise characteristics. No perfect compensation, however, is possible. Thus, in spite of various improvements, the main disadvantage of the fractional-N technique is the excessive spurious levels produced by phase errors inherent in the fractional division mechanism.

## SELF-OFFSET SCHEME

From the first glance, alternating frequency division coefficients seems to be a "natural" way to obtain fractional-N values. This is not necessarily true. Fractional division coefficients can be realized by other means that can avoid changing division ratios on the fly. An interesting scheme (called a "self-offset loop") has been presented by Sadowski.[12] The scheme utilizes a mixer in the PLL feedback path as depicted in ***Figure 2***. The mixer inputs are generated internally within the same PLL, therefore, no separate offset frequency source is required. Two frequency dividers (having division ratios A and B) divide the VCO output frequency to generate the required mixer inputs. It is easy to show that $f_{out} = f_{REF} \frac{AB}{A \pm B}$, thus, this scheme allows fractional division coefficients.

Let's examine how this circuit works. Imagine that we need to synthesize a signal at 119 MHz using a 10 MHz reference. If we use a conventional integer-N PLL approach, first we would need to divide the reference down to 1 MHz at the phase detector input. Then we would generate the required output by setting the division ratio in the PLL feedback path

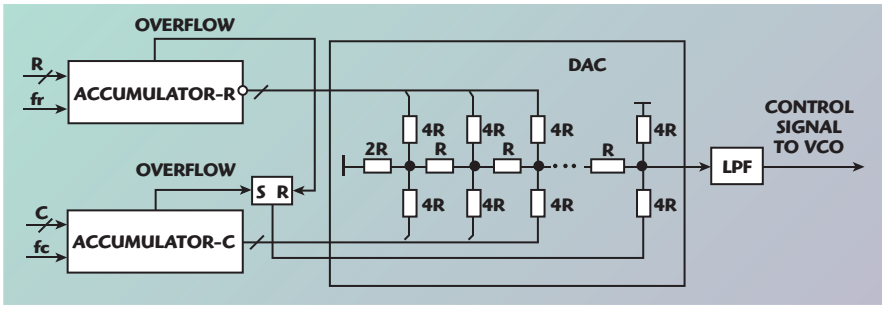



*Fig. 3 Phase comparison with unequal frequency inputs and analog processing.*



to 119. This results in over 41.5 dB phase noise degradation. We can obtain the same output frequency in the self-offset scheme by setting division coefficients to A=17 and B=7. The dividers generate two mixer inputs at 7 and 17 MHz, respectively, thus, their difference (filtered at the mixer output) of 10 MHz is compared with the reference frequency. Note that we have essentially realized the fractional division ratio of 11.9 that results in substantial phase noise improvement compared to the conventional integer-N PLL. A disadvantage of such a structure is the need to select properly required division coefficients and filter out undesired mixer products.

## PHASE COMPARISON WITH UNEQUAL INPUTS

Conventional wisdom suggests that the heart of any PLL should be a phase detector that compares two equal frequencies at its inputs to close the loop. Bosselaers looked at this from a slightly different angle.[13] He has proposed a circuit that consists of two accumulators clocked by the reference fr and signal fc frequencies, respectively. It also includes an arithmetic unit that digitally adds and subtracts current states of the accumulators. The result is transformed by a DAC into analog equivalent to control a VCO. When the total of the additions of the number R equals to the total of the subtractions of the number C over a period of time, the output frequency will be set to fc = fr R/C, where R and C are numeric values of the codes at the control inputs of corresponding accumulators. In general, the R and C values are not equal; therefore, the circuit provides the opportunity for phase comparison of unequal, fractionally-N related frequencies. The main drawback of this idea is that there is an uncertainty state when fc and fr pulses coincide. This results in a glitch and, thus, significant degradation of the signal spectrum.

Koslov has further improved this concept by processing the accumulator outputs with analog means to avoid the accumulator output uncertainty issue.[14] There are two identical accumulators R and C clocked by fr and fc signals, respectively. The accumulator outputs (one of them is inverted) are summed in a special DAC represented

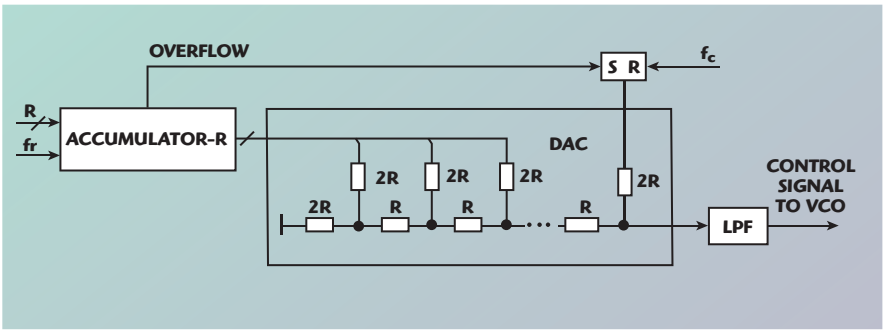



*Fig. 4 Phase comparison using a single accumulator.*



by a resistive ladder network as shown in ***Figure 3***. The most significant bit of the DAC operates from an RS-flip-flop switched by the overflow pulses coming from the accumulators. This scheme can be further simplified[15] by eliminating one of the accumulators, as depicted in ***Figure 4***. The second accumulator is excluded since its control code is fixed and, thus, its function is reduced to sending the signal pulses to the input of the RS-flip-flop.

## PHASE SPLITTING

Synthesizer characteristics can be significantly improved using the idea of phase splitting.[16] To illustrate the concept, let's assume that there are voltage glitches in a PLL circuit (as shown in ***Figure 5***) represented by short pulses on the diagram A. Let's move these pulses by 1, 2 and 3 clocks and then sum them together with equal weights of 1/K (where K is 4 in this case) as illustrated on the diagram B of the same figure. Obviously, the amplitude of the resulting pulses is decreased four times although its average DC power remains the same. The diagram C shows the case when the shifts are 2, 4 and 6 clocks and the diagram D corresponds to the shifts of 8, 16 and 24 clocks, respectively. Note that in the latter case not only the amplitude but repetition frequency changes (increases). Thus, it may be easier to filter out these glitches.

This concept requires several partial phase detectors that are properly phased in respect to each other. One practical implementation called phase digital synthesizer is presented in references 17 and 18. The proposed solution consists of two channels (representing the reference and signal paths) that include accumulators (R-Acc and C-Acc) and phase splitters (R-PS and C-PS) as depicted in ***Figure 6***. The phase splitters drive partial phase detectors constructed with RS-flip-flops and a DAC as discussed earlier. For additional spur compensation, some least significant bits of the accumulators are optionally connected to R2R-sections of the DAC. In the signal path, they may be only required to select a preferable combination of codes R and C to tune out some troublesome spurs such as integer boundary spurs. The outputs of the partial phase detectors are pro-

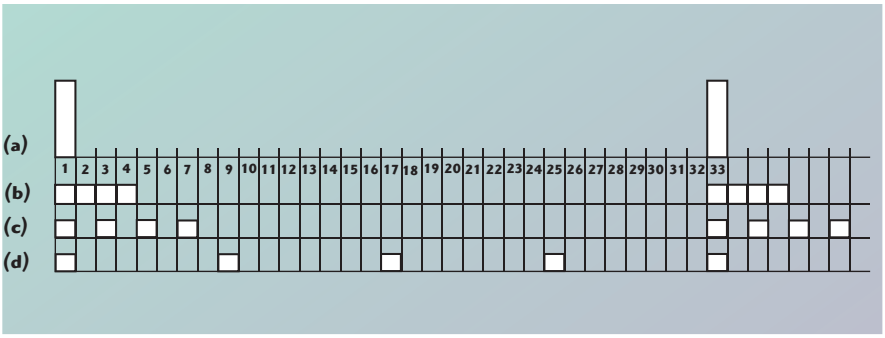



*Fig. 5 Phase splitting concept.*



cessed in a DAC that generates a VCO control voltage. An ideal DAC would have only a DC component (for controlling the VCO frequency) and two saw-tooth components with frequencies fr and fc, which are filtered out by the loop filter. In reality, some spur degradation occurs due to DAC errors.

The essence of the presented phase digital synthesizer is that the control signal of the PLL is formed by a multi-phase comparator with phase splitting of the reference and VCO signals into a large number of partial channels. Another interesting feature is that phase comparison takes place directly at the clock frequencies, thus reducing frequency multiplication within the loop. Overall, spectral purity characteristics heavily depend on the number of partial phase detectors as well as DAC accuracy. The analysis presented in reference 18 shows quite superior performance compared to conventional fractional-N techniques. The solution is particularly well suited for implementation as an IC that allows constructing a large number of partial channels for better spectral characteristics. Building this circuit on a single chip can support the on-going demand for low-cost, high-performance frequency synthesizers.

This article highlights just a few interesting ideas that can potentially move current technology barriers. Can they be practically used? Some ideas thrive while others die. According to statistics, not more than 2 percent of patents are implemented in practice. Much of the value of looking at a problem from another person's point of view is that it helps us recognize and compensate for our own biases. Changing a perspective is a very valuable tool to develop new products. ■

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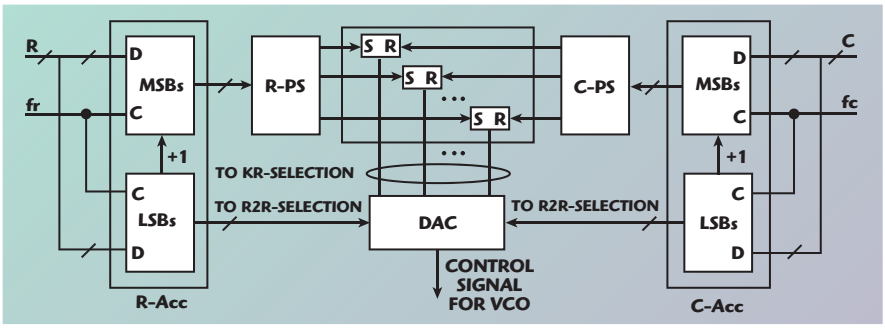


▲ *Fig. 6 Phase digital synthesizer.*



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