A 26.5 GHz PLL Synthesizer with Low Phase Noise Characteristics

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***Abstract* — A novel PLL frequency synthesizer architecture is presented. The proposed architecture offers improved phase noise characteristics by removing frequency division from the PLL feedback path. This minimizes the impact of the phase detector residual noise floor. Moreover, phase noise can be further improved by inserting a frequency multiplier into the feedback path. A 5 MHz to 26.5 GHz synthesizer module based on the proposed architecture has been developed. Phase noise at 26.5 GHz output and 10 kHz offset is measured at –110 dBc/Hz. The measured spurs do not exceed -60 dB level. The switching time is less than 100 microseconds for any frequency step within the entire operating range.**

***Index Terms* — Frequency divider, frequency synthesizer, noise floor, phase detector, phase noise, voltage-controlled oscillator.**

I. Introduction

A phase-lock-loop (PLL) frequency synthesizer is key building block, which has been extensively used in RF and microwave systems [1]-[3]. A generic single-loop PLL synthesizer block diagram is shown in Fig. 1. It includes a tunable voltage-controlled oscillator (VCO) that generates a signal in a desired frequency range. This signal is fed back to a phase detector through a frequency divider with a variable frequency division ratio *N*. The other input of the phase detector is a reference signal equal to a desirable step size. The phase detector compares the signals at both inputs and generates an error voltage, which following filtering and optional amplification, slews the VCO until it acquires the lock frequency given by

$$f_{OUT} = N f_{PD} \qquad (1)$$

where f_{PD} is the comparison frequency at the phase detector inputs.

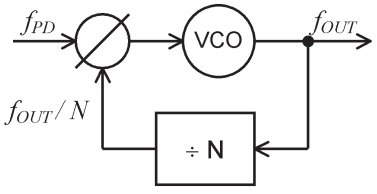

Fig. 1. A block diagram of a generic single-loop PLL synthesizer.

The phase noise outside the PLL filter bandwidth is mainly determined by the VCO's free-running noise. The phase noise within the loop filter bandwidth is given by

$$\mathcal{L}_{PLL} = \mathcal{L}_{\Sigma PD} + 20\log N \qquad (2)$$

where $\mathcal{L}_{\Sigma PD}$ is the cumulative phase noise at the phase detector input. At low frequency offsets (e.g., 10 Hz to 100 Hz), the reference noise usually dominates and, thus, translates to the synthesizer output almost at the "ideal" *20logN* rate. At higher frequency offsets, the phase detector noise becomes a dominant factor. Hence, a lot of research has been focused on reducing phase detector residual phase noise characteristics. Note that one naturally assumes that $N>1$; therefore, the phase detector noise is degraded by large division ratios required to provide a high-frequency output with a fine resolution. However, as a more general case, three scenarios are possible as follows:

1. $N>1$, phase detector noise is degraded by *20logN*
2. $N=1$, phase detector noise is not degraded
3. $N<1$, phase detector noise is improved by *20logN*

The scenario 1 describes a "classical" single-loop PLL as depicted above. The scenario 2 assumes removing the frequency divider from the PLL feedback path, thus, eliminating phase noise degradation. The scenario 3 can be implemented by inserting a frequency multiplier instead of the frequency divider that further improves phase noise [4]. This paper discusses a block diagram and practical implementation of such a method of PLL phase noise reduction.

II. Synthesizer Architecture

A general block diagram of the proposed synthesizer core is shown in Fig. 2. The VCO output signal *f* is converted in mixers M_1-M_i to the phase detector comparison frequency F_0 equal to the synthesizer step size. The comparison frequency as well as mixer LO signals $f_1 \ldots f_i$ are produced from a common, highly stable, low phase noise reference signal F_{REF} using frequency dividers with frequency division ratios D_1-D_i and frequency multipliers with multiplication factors C_1-C_i respectively. The multiplier can be comb generator, whose output contains a large number of harmonics.

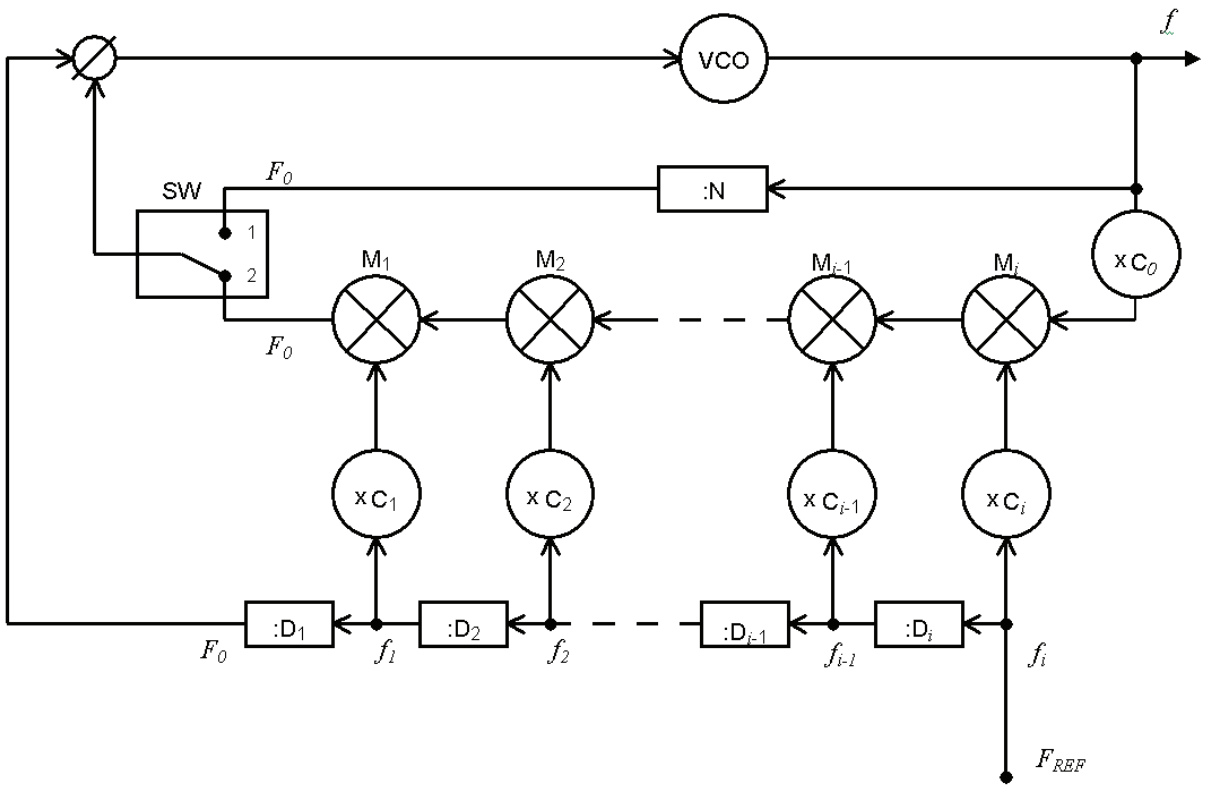

Fig. 2. A general synthesizer architecture.

First, assume that the multipliers are not utilized (i.e., C_0=C_1=⋯=C_i=1). The phase detector compares the signals at both inputs and generates an error voltage which slews the frequency of the VCO to a lock frequency given by

$$f = f_i \pm f_{i-1} \pm \ldots \pm f_2 \pm f_1 \pm F_0 \qquad (3)$$

that, after simple manipulations, leads to

$$f = F_0\left(D_1D_2\ldots D_{i-1}D_i \pm D_1D_2\ldots D_{i-1}\right) \pm \ldots$$

$$\ldots \pm F_0\left(D_1D_2 \pm D_1 \pm 1\right). \qquad (4)$$

Since all the division coefficients are integer numbers, we can write

$$f = F_0\, N \qquad (5)$$

where

$$N = D_1D_2\ldots D_{i-1}D_i \pm D_1D_2\ldots D_{i-1} \pm \ldots$$

$$\ldots \pm D_1D_2 \pm D_1 \pm 1 \qquad (6)$$

is an integer.

Therefore, the VCO can be locked at a large number of equally spaced output frequencies. In other words, the synthesizer is capable of generating precise frequencies within the VCO operating range with the step size equal to F_0.

A desired output frequency can be chosen using an additional coarse-tuning divider with a programmable division ratio N inserted into the synthesizer loop with the help of a switch SW (Fig. 2). Initially the switch is in the upper position connecting the divider. The circuit works as a conventional single-loop PLL brining the VCO output to the desired frequency. Thus, the divider provides a simple and reliable mechanism to pre-tune the VCO to exactly the correct frequency. This mechanism does not depend on the VCO temperature drift or any other component variations. Then the switch SW turns off the divider feedback path and connects the mixer chain to ensure that no phase noise degradation occurs.

One advantage of this scheme is that the mixers do not generate undesired products within the synthesizer loop bandwidth. The output of every mixer includes a vast number of products, including the fundamentals of the mixer's RF and LO signals and their harmonics, and the sums and differences of the RF and LO and their harmonics given by

$$f_{MIX} = \pm m f_{RF} \pm n f_{LO} \qquad (7)$$

which can be written for the mixer M_i as

$$f_{MIX\,i} = \pm mF_0 N \pm nF_0 D_1 D_2 ... D_{i-1} D_i . \qquad (8)$$

Assuming that all the coefficients are integers, the mixer products are given by

$$f_{MIX\,i} = k F_0 \qquad (9)$$

where k is an integer number. Similarly, it can be shown that all harmonic and intermodulation products generated by the mixer chain are multiples of the phase detector frequency F_0, which can be easily rejected by the loop filter. The frequency tuning algorithm is summarized as follows:

1. A required output frequency *f* is determined.
2. The switch is initially in the position 1 (Fig. 2). The coarse-tuning divider is connected; the mixer chain is disconnected.
3. The divider ratio is programmed to *N* equal to the ratio between the required output frequency *f* and resolution F_0.
4. The phase detector generates a voltage required to bring the VCO output to the desired output frequency *f*.
5. The phase detector also generates a lock detection signal turning the switch to the position 2, thus, removing the divider from the loop. The mixer chain is turned on.
6. The output signal *f* is converted in the mixer chain to substitute the phase detector comparison frequency F_0 generated initially by the divider.
7. The phase detector relocks the output signal with no frequency division within the loop ensuring low phase noise operation.
8. The loop filter cleans up undesired mixer products providing low spurious operation.

Insertion of frequency multipliers results in other mixer products that will be investigated in further publications. However, the concept of phase noise reduction remains the same. Note that phase noise performance can be further improved by inserting the frequency multiplier C_0 into the PLL feedback path as also depicted in Fig. 2. Just as frequency division in the PLL feedback path increases phase noise by *20logN*, frequency multiplication reduces phase detector noise by the same factor. Therefore, insertion of the frequency multiplier C_0 results in lower phase noise output (assuming that phase detector noise dominates). A trade-off associated with this scheme is coarser resolution that can be controlled by introducing a larger number of mixer stages.

III. Module Design

A simplified block diagram of the developed synthesizer module is presented in Fig. 3. The main PLL block includes a fundamental VCO covering the 10-to-20 GHz frequency range. The reference signal F_{REF} is created with another PLL block that also includes a DDS to fill in the gaps between the main PLL steps. The DDS spurs are suppressed with a combination of software and hardware (upconversion followed by division) techniques as discussed in more detail in [5]. A frequency resolution of 0.001 Hz is achieved. The frequency coverage above 20 GHz is provided with a frequency multiplier. Since the multiplied bandwidth is relatively narrow (less than an octave), subharmonic filtering is achieved with a single filter path (i.e., no switch filter bank is needed). The frequency coverage below 10 GHz is provided with a programmable divider. The full frequency coverage is 5 MHz to 26.5 GHz. The synthesized signal level is controlled using a built-in variable gain attenuator.

The synthesizer is built on a printed circuit board that is placed into a metal enclosure measuring 7 by 5 by 1 inches in dimensions as shown in Fig. 4. The module can be controlled through SPI and USB interfaces, which are realized with a built-in processor.

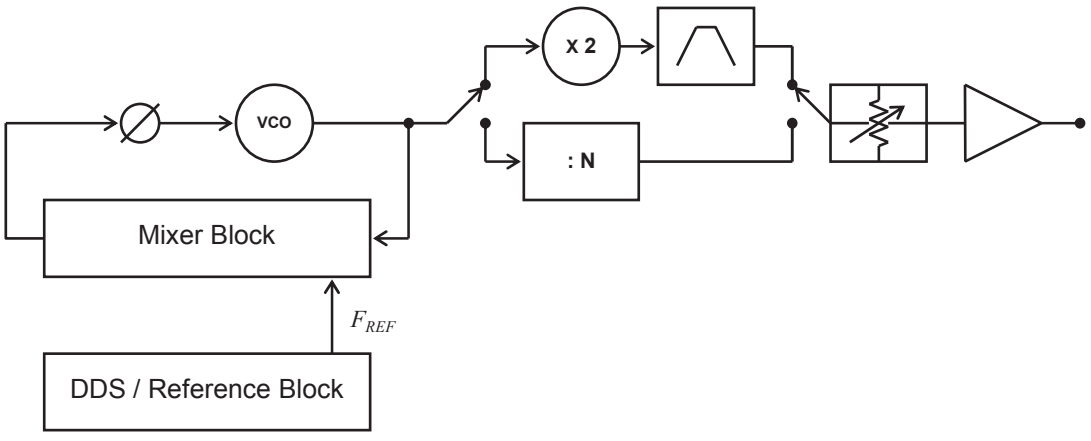

Fig. 3. A synthesizer block diagram.

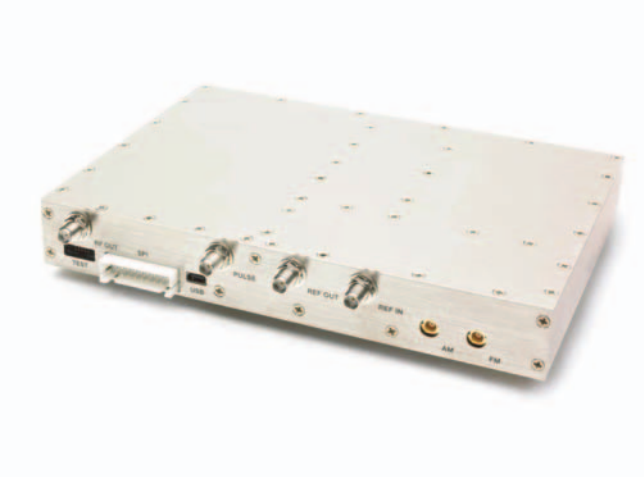

Fig. 4. Developed synthesizer module.

IV. Test Data

The synthesizer can be tuned between 5 MHz and 26.5 GHz with a 0.001 Hz step. The output power is +10 dBm and is fairly flat across the entire operating range. This is achieved by storing control voltage constants during calibration process. As a result, the power variations do not exceed ±1 dB. The phase noise plot taken at 26.5 GHz is presented in Fig. 5. The measured phase noise at 10 kHz offset is about -110 dBc/Hz. The phase noise at lower output frequencies improves at 6 dB per octave rate until it reaches the residual noise floor of the utilized divider. For example, the phase noise at the 10 MHz output is shown in Fig. 6. Further improvements at low frequencies are expected with lower noise floor frequency dividers.

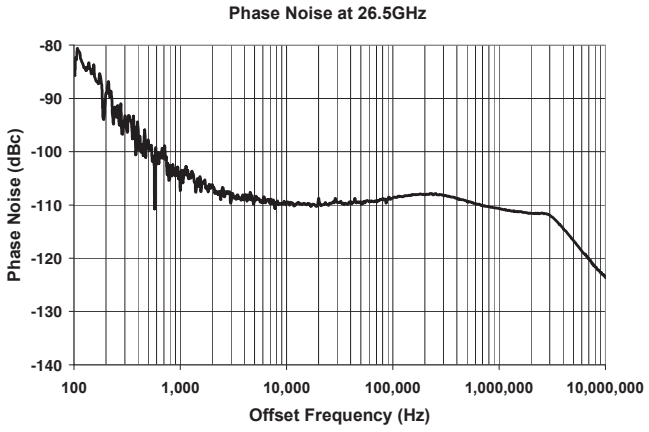

Fig. 5. Phase noise at 26.5 GHz.

The measured spurs do not exceed -60 dB level. The switching time is less 100 microseconds for any frequency step within the entire operating range (to be within ±50 kHz of the destination frequency). This speed is achieved due to the utilized VCO and very wide (a few MHz) loop filter bandwidth. The module is biased from a single +12V DC supply. The overall DC power consumption does not exceed 20 Watts.

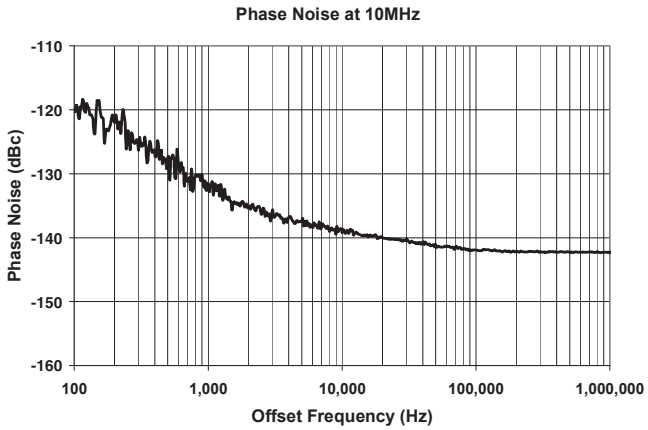

Fig. 6. Phase noise at 10 MHz.

V. Conclusions

A novel PLL synthesizer architecture and frequency tuning method have been discussed. The proposed architecture has several advantages as follows:

1. A simple, reliable, and exact coarse-tuning mechanism, which does not depend on component instabilities.
2. Low spurious performance due to the absence of undesired products within the loop bandwidth.
3. Low phase noise performance due to removing frequency dividers from the synthesizer loop.

A 5 MHz to 26.5 GHz synthesizer based on the proposed architecture has been developed. The synthesizer demonstrates excellent phase noise and switching speed characteristics. This developed module can be used in a variety of applications where a broadband coverage, low phase noise, and fast switching speed characteristics are required.

References

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