Broadband PXI Local Oscillator Modules with Low Phase Noise and Fast Switching Speed

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***Abstract*—This paper presents two local oscillator modules developed for PXI instrumentation. The modules are based on a novel, patented PLL design that combines fast switching speed, low phase noise, and low spurious characteristics. The modules cover 3-10 and 2-20 GHz frequency ranges respectively. The step size is 0.1 Hz for both modules. The measured phase noise at 10 kHz offset is about –121 dBc/Hz at 10 GHz and -115 dBc/Hz at 20 GHz respectively. The switching time is less than 500 microseconds to be within ±50 kHz from the final frequency for any frequency step within the entire operating range. Spurs do not exceed the –70 dBc level. Both developed modules occupy two standard 3-U PXI slots and can be used in a variety of synthetic instruments based on the PXI platform.**

Keywords-synthetic instrument; PXI module; frequency synthesizer; local oscillator; microwave source; phase noise; switching speed

I. INTRODUCTION

PXI synthetic instrumentation offers a cost-effective modular approach for building complex test-and-measurement equipment [1-2]. The performance of synthetic instruments primarily depends on technical characteristics of their core modules. The frequency synthesizer is one of the key elements of virtually any RF/microwave system. It generates a stimulus signal or is used as a local oscillator (LO) in a variety of up- and down-conversion schemes. Thus, the industry feels persistent pressure to deliver higher-performance synthesizer designs.

The ideal synthesizer should be broadband with a fine frequency resolution that allows addressing a wider range of potential applications. Aside from frequency coverage and resolution, phase noise and spurious content are critical parameters that impose the ultimate limit in the system's ability to resolve signals of small amplitude. This is an important consideration in spectrum analysis applications. Another key parameter of the synthesizer that impacts overall system performance is the frequency switching speed [3-4]. The time spent by the synthesizer transitioning between frequencies becomes increasingly valuable since it cannot be used for data processing. While many systems still work adequately with millisecond switching speeds, newer requirements demand microsecond operation along with the good spectral purity of traditional lower-speed designs.

There are several approaches to generate clean output signals; however, there is typically a tradeoff between switching speed and phase noise. Historically, high-performance microwave signal generators have relied on YIG-tuned oscillators featuring broadband operation and excellent phase noise characteristics [5]. However, YIG oscillators exhibit several drawbacks including high power consumption, large physical size, and – more importantly – slow tuning speed due to the presence of a high-inductance tuning coil. An alternative solution is the use of VCOs, which are currently available in small surface-mount packages. VCO-based synthesizers are significantly faster; however, their phase noise has traditionally been considered to be inferior when compared to YIG-based designs.

We previously introduced a VCO-based PXI LO module that covered the 3-9 GHz frequency range with 0.1 Hz resolution and better than 1 millisecond switching time [6]. However, the phase noise of about -90 dBc/Hz at 9 GHz output and 10 kHz offset restricted its use in phase noise-sensitive applications such as spectrum analysis. Furthermore, operation at higher frequencies was also desired. These requirements initiated the development of new PXI LO modules to achieve a wider frequency coverage and better phase noise.

We discuss here an innovative design approach that provides a unique combination of fast-switching speed and very low phase noise characteristics. Two local oscillator modules covering the 3-10 and 2-20 GHz frequency ranges will be presented.

II. DESIGN CONCEPT

The main idea in the development of new LO modules is to substitute a slow-tuning, bulky, and expensive YIG oscillator (normally used in high-performance signal generator designs) with a tiny VCO that can easily support microsecond tuning. Excessive phase noise (traditionally associated with VCO devices) is suppressed by utilizing a very wideband phase-lock-loop (PLL) scheme in conjunction with a low-noise reference source. To illustrate this approach, let's compare phase noise behavior of two hypothetical oscillators (YIG and VCO) that utilize identical active device arrangements. The oscillator noise behavior can be represented with a well-known modification of Leeson's equation [7-8] that depicts the oscillator phase noise behavior in the offset frequency domain as follows:

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$$\mathcal{L} \approx 10\log\left\{\frac{GFkT}{2P}\left[\left(\frac{f_0}{2Q}\right)^2 \times \frac{f_c}{f^3} + \left(\frac{f_0}{2Q}\right)^2 \times \frac{1}{f^2} + \frac{f_c}{f} + 1\right]\right\}$$

where

G = active device gain

F = active device noise factor

k = Boltzmann's constant

T = absolute temperature

P = RF power applied to the resonator

Q = resonator loaded Q-factor

f_0 = oscillation frequency

f_c = active device flicker-corner frequency

f = offset frequency

Although the formula defines four basic frequency offset regions, in microwave oscillators the $1/f$ term is ignored because of the $1/f^2$ noise domination. This leads to the "classical" microwave oscillator phase noise profile shown in Fig. 1. At very high frequency offsets, both oscillators should demonstrate the same behavior (noise floor) defined by the ratio of the available RF power and thermal noise of the active device. The noise starts degrading at a rate of 20 dB per decade at lower frequency offsets. The degradation start point is defined by the Q-factor of a utilized resonator. In the last region, where the flicker noise dominates, the phase noise increases at 30 dB per decade. Clearly, the VCO demonstrates significantly higher phase noise in comparison with the YIG-oscillator because of the difference in their resonator Q-factors.

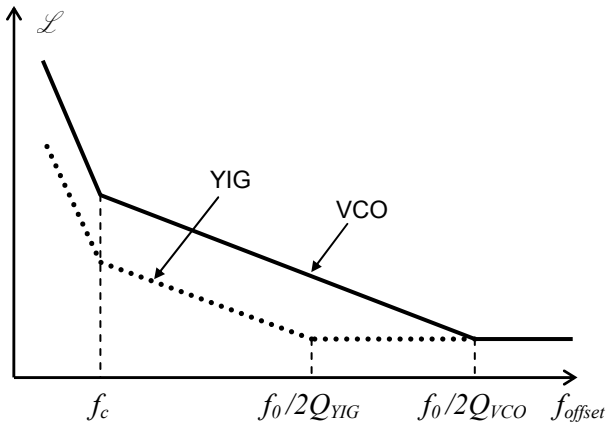

Figure 1. Phase noise behaviour of VCO and YIG oscillators.

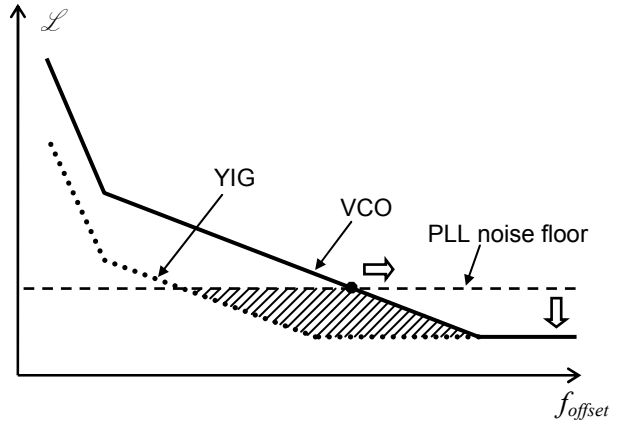

Figure 2. Reducing the PLL noise floor and widening the loop filter bandwidth minimize the difference in phase noise between YIG and VCO-based synthesizers.

Now let's build a synthesizer using these oscillators or, in other words, lock them to a low-noise reference source. What phase noise behavior is expected? The answer obviously depends on the available reference noise characteristics, PLL residual noise floor, and the loop filter bandwidth. The loop filter bandwidth is preferably set to its optimal frequency (which is the cross point of the PLL multiplied noise and oscillator free-running noise curves) that provides the lowest overall phase noise response. Since the VCO is now locked within a wider loop bandwidth, it locks much faster than the YIG. However, the VCO phase noise curve is still well above the YIG counterpart. The difference in phase noise between the YIG and VCO-based synthesizers is set by the PLL noise floor and free-running oscillator noise curves and is indicated as a hatched area in Fig. 2. Predictably, reducing the PLL noise floor and simultaneously widening the loop filter bandwidth minimizes the difference, thus, making a VCO-based synthesizer behavior similar to its YIG counterpart.

Can a VCO-based design achieve YIG-comparable performance? Let's take a look from another side. Assuming that we have an ideal, noiseless PLL mechanism, the reference noise is translated at *20logN* rate where *N* is PLL multiplication factor. Therefore, the output phase noise is still limited by the available reference that becomes a dominating factor. Today's commercial crystal oscillators can perform within -160 to -180 dBc/Hz at 10-kHz offset at 100-MHz output. These numbers can be potentially translated to -120 to -140 dBc/Hz at 10 GHz, which corresponds or even supersedes the performance of the best YIG oscillators at the same frequency settings.

In practice, the noise limitations are mainly set by PLL residual noise characteristics or, in other words, by a particular synthesizer architecture. The key principles in designing low-noise, fast-switching, VCO-based PLL synthesizers are briefly summarized as follows:

- using a very low-noise reference source
- reducing PLL residual noise floor
- extending the loop filter bandwidth

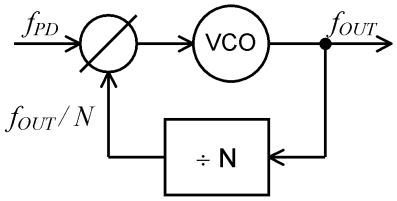

Figure 3. A block diagram of a generic single-loop PLL synthesizer.

Thus, the key consideration in our new design is how to reduce the PLL noise floor. In contrast to traditional architectures (which tend to minimize the PLL division ratio), this new approach makes a more radical step by completely removing the divider from the loop. Moreover, it inverts the PLL division ratio by applying a multiplication within the PLL that drastically improves both phase noise and spurious characteristics.

This concept is illustrated in Fig. 3 that shows a generic single-loop PLL synthesizer block diagram. The PLL includes a tunable VCO that generates a signal in a desired frequency range. This signal is fed back to a phase detector through a frequency divider with a variable frequency division ratio *N*. The other input of the phase detector is a reference signal equal to a desirable step size. The phase detector compares the signals at both inputs and generates an error voltage, which following filtering and optional amplification, slews the VCO until it acquires the lock frequency given by

$$f_{OUT} = N f_{PD}$$

where f_{PD} is the comparison frequency at the phase detector inputs. The phase noise outside the PLL filter bandwidth is mainly determined by the VCO's free-running noise. The phase noise within the loop filter bandwidth is given by

$$\mathcal{L}_{PLL} = \mathcal{L}_{\Sigma PD} + 20\log N$$

where $\mathcal{L}_{\Sigma PD}$ is the cumulative phase noise of the reference and phase detector. At low frequency offsets (e.g., 10 Hz to 1 kHz), the reference noise usually dominates and, thus, translates to the synthesizer output almost at the "ideal" *20logN* rate. However, at higher frequency offsets, the phase detector noise becomes a dominant factor. Hence, a lot of research effort has been focused on reducing phase detector residual phase noise characteristics. Note that one naturally assumes that *N*>1; therefore, the phase detector noise is degraded by large division ratios required to provide a high-frequency output with a fine resolution. As a more general case, three scenarios are possible as follows:

$N > 1$, phase detector noise is degraded by *20logN*

$N = 1$, phase detector noise is not degraded

$N < 1$, phase detector noise is improved by *20logN*

The scenario 1 describes a "classical" single-loop PLL as depicted above. Scenario 2 assumes removing the frequency divider from the PLL feedback path, thus, eliminating phase noise degradation. The Scenario 3 can be implemented by inserting a frequency multiplier instead of the frequency divider that further improves phase noise [9]. Interestingly, these measures (i.e., loop division reduction and inversion) also work well for spur reduction. This is based on the fact that phase noise can be thought of randomly distributed spurs. This design concept has been first utilized in a "brick" module synthesizer (also known as QuickSyn™) and has successfully demonstrated its exceptional efficiency in terms of low phase noise and fast tuning speed as discussed in detail in [10-11]. The concept is now applied in the design of new modules in the PXI form factor.

III. Module Construction

Two PXI local oscillator modules PXI-1450B and PXI-1550 (covering the 3-10 and 2-20 GHz ranges respectively) have been constructed. The modules have the same form factor occupying two standard 3-U PXI slots and also have the identical front panel as shown in Fig. 4.

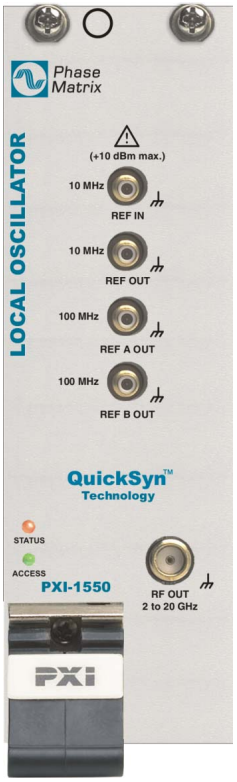

Figure 4. A developed PXI LO module.

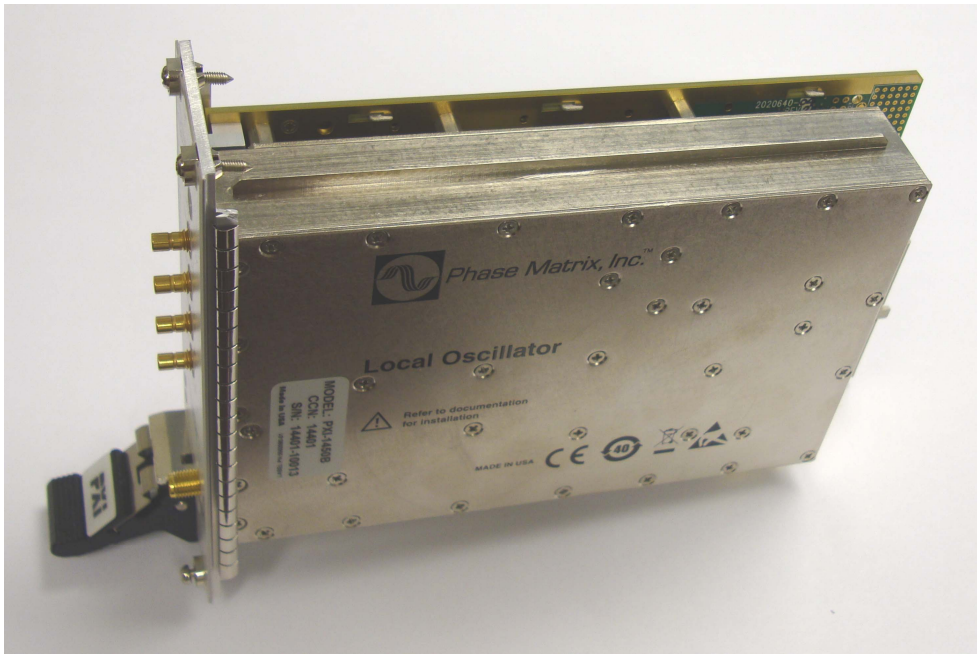

Figure 5. RF/microwave circuits are completely shielded in a metal housing.

The front panel includes an SMA connector that outputs the synthesized signal in the 2-20 (as shown) or 3-10 GHz frequency ranges. There are also four SMB connectors that handle reference signals for the module synchronization with other PXI components. The synthesizer includes a highly-stable, low phase noise 100 MHz OCXO that is used as an internal time base. Two 100 MHz outputs are derived from this OCXO and are available for external use. The module includes a built-in divider-by-10 that presents a 10 MHz signal normally used for external equipment synchronization. Furthermore, the internal OCXO can be locked to an external 10 MHz reference signal as needed. Two LED indicators monitor proper operation and communication of the module within the PXI environment.

IV. Control Interface

The RF/microwave circuits are completely shielded in a metal housing (as shown in Fig. 5) to prevent interference from the outside environment and possible signal contamination. The RF/microwave block also includes a built-in 32-bit, 200 MHz CPU that brings the required horsepower to support all necessary frequency tuning calculations on the fly. It also includes non-volatile memory to store all necessary calibration constants. This drastically simplifies unit calibration and control. Two parameters are calibrated as follows:

- internal reference (time base) accuracy

- RF output power versus output frequency

A PXI interface board is placed on top of the housing to deliver all bias voltages and control signals from a PXI chassis. The connection between the PXI interface board and the RF/microwave block is provided via an internal SPI interface. The whole module is controlled through the PXI bus with a LabView GUI, which is hosted on an external computer. The GUI (Fig. 6) allows the user to set a desired output frequency, monitor frequency lock, and mute the synthesizer output as required. The user can mute the 10 MHz reference output, monitor the presence of an external 10 MHz signal, and check the reference lock. The software also allows sweeping the synthesizer across the entire frequency range with programmable frequency step and dwell time.

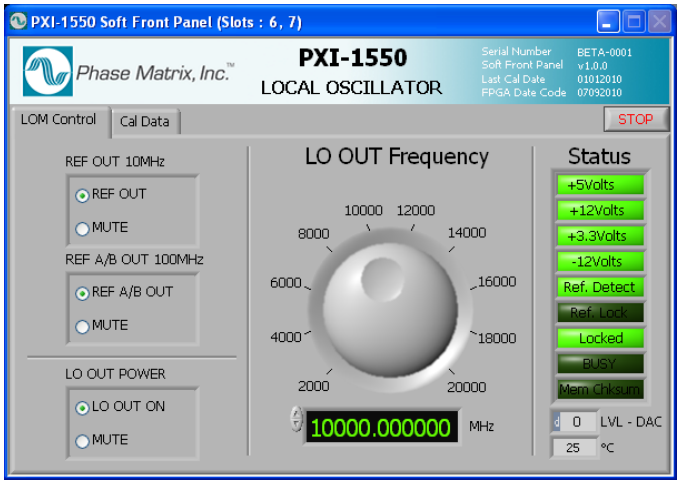

Figure 6. Module control.

V. MEASUREMENTS

Both modules exhibit nearly identical technical characteristics. The main difference is the operating frequency range of 3-10 and 2-20 GHz respectively. The step size is 0.1 Hz in both cases. The output power is calibrated at +15 dBm and remains flat within ±1 dB within the entire operating frequency range. The design also includes sophisticated temperature compensation resulting in repeatable output power characteristics across the operating temperature range. The output power can be turned off (i.e., muted) by switching off the output power amplifier. Note that the VCO and PLL core remain turned on, which minimizes recovery time when the synthesizer is back to normal operation.

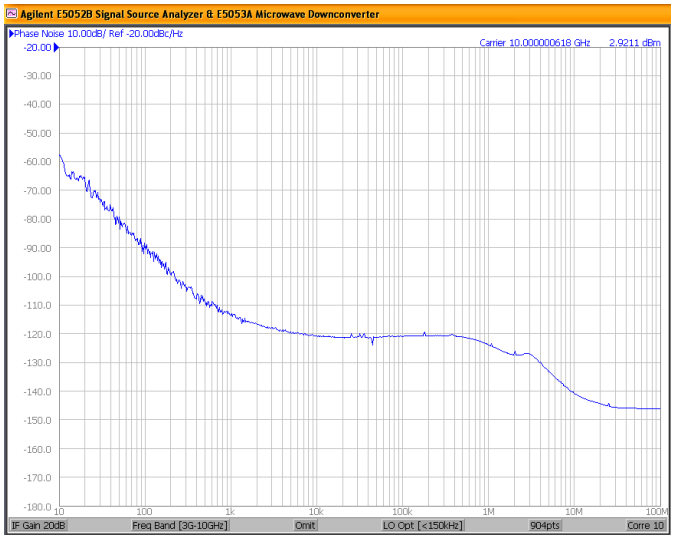

Figure 7. Phase noise at 10 GHz.

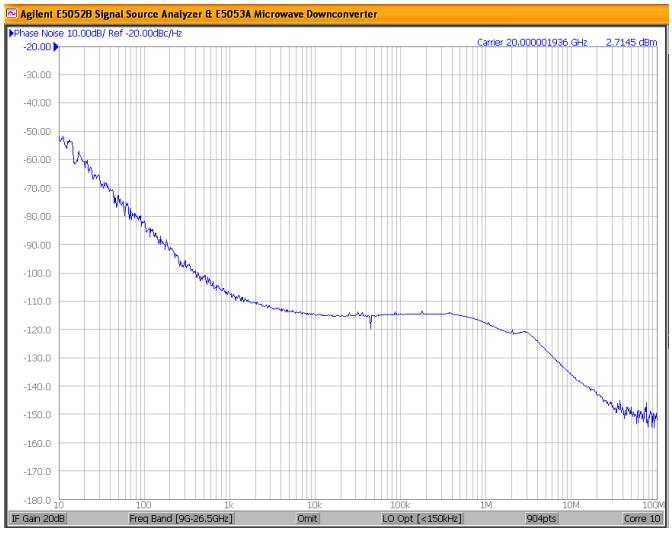

Figure 8. Phase noise at 20 GHz.

The overall switching time (including all internal calculations) is less than 500 microseconds to be within ±50 kHz from the final frequency. This speed is supported for any frequency step within the entire operating range.

Phase noise plots at 10 and 20 GHz are presented in Fig. 7 and Fig. 8 respectively. The phase noise at 10 kHz offset is about –121 dBc/Hz at 10 GHz and –115 dBc/Hz at 20 GHz respectively. Phase noise at lower frequencies further reduces at 6 dB per octave rate due to the employed frequency division architecture. Spurs do not typically exceed the –70 dBc level. Spur measurements are taken at 10 GHz and frequency spans of 10 MHz and 10 kHz as illustrated in Fig. 9 and Fig. 10 respectively.

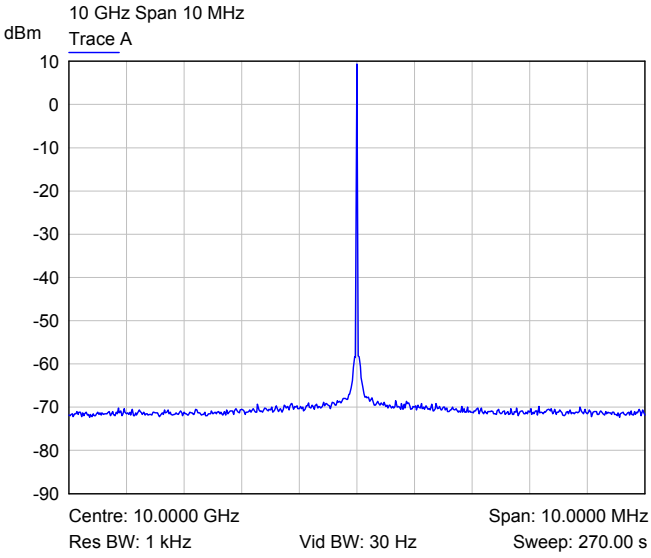

Figure 9. Spurs at 10 GHz with 10 MHz span.

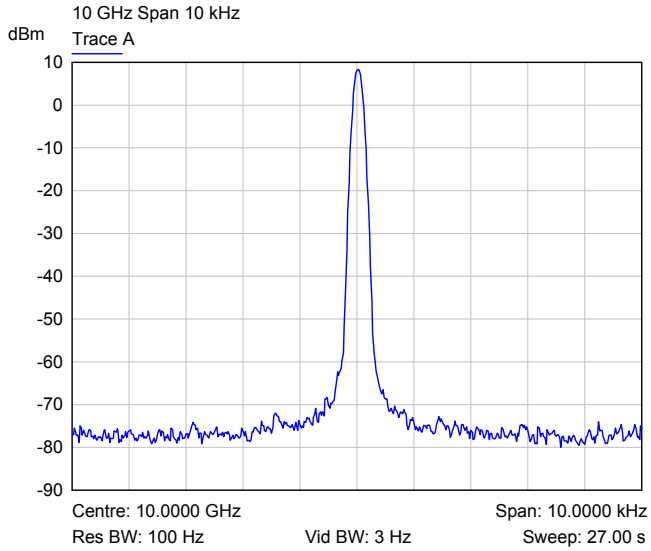

Figure 10. Spurs at 10 GHz with 10 kHz span.

VI. CONCLUSIONS

Two PXI LO modules have been developed. The modules are based on a novel, patented PLL design that combines fast switching speed, low phase noise, and low spurious characteristics. A brief summary of the LO modules key parameters is depicted in Table. 1.

TABLE I. PXI LO MODULES PERFORMANCE SUMMARY

Parameter	Measurement
Frequency Range	3-9 and 2-20 GHz
Step Size	0.1 Hz
Output Power	+15 dBm
Switching Time	500 usec
Phase Noise at 10 kHz offset	-115 dBc/Hz at 20 GHz -121 dBc/Hz at 10 GHz
Spurs at 10 GHz	-70 dBc

The modules cover the 3-10 and 2-20 GHz frequency ranges. The step size is 0.1 Hz for both modules. The switching time to ±50 kHz accuracy is less than 500 microseconds for any frequency step within the entire operating ranges. The phase noise at 10 kHz offset is about –121 dBc/Hz at 10 GHz and –115 dBc/Hz at 20 GHz respectively. The measured spurs do not exceed the –70 dBc level.

Remarkably, these characteristics are achieved by using low-cost, general-purpose ICs, which are offered as standard "of-the-shelf" parts. This has resulted in a compact design as required to fit into PXI form factor constraints. Both developed modules occupy two standard 3-U PXI slots and can be used in a variety of synthetic instruments based on the PXI platform.

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