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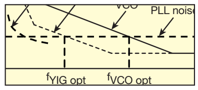

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AMPLIFIERS & OSCILLATORS ISSUE

YIGs or VCOs in PLLs?

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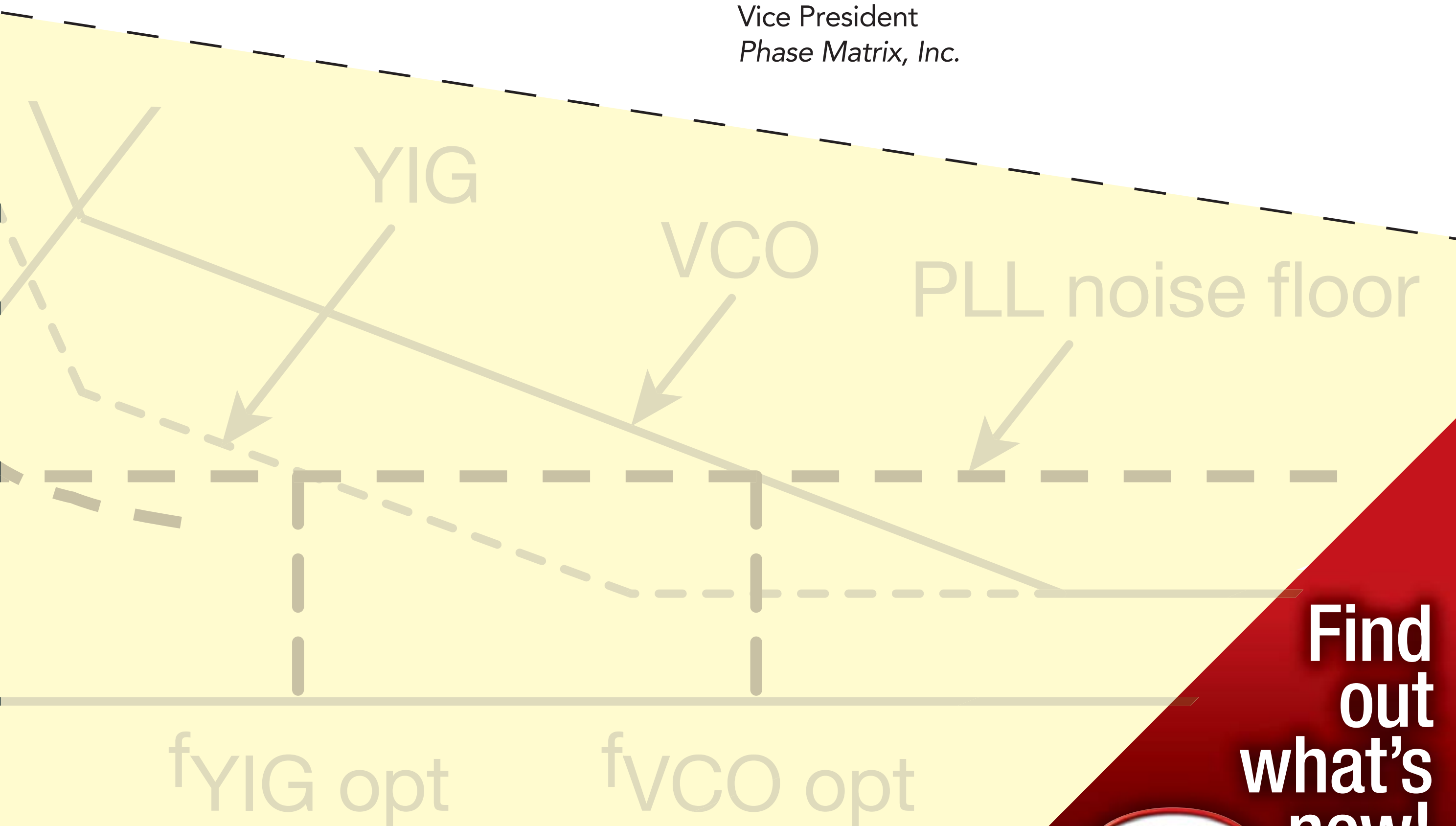
Phase Matrix, Inc.



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Select A VCO or YIG For A PLL Synthesizer?

Using advanced wideband PLL architectures, a low-cost, fast-switching voltage-controlled oscillator (VCO) offers an excellent alternative to commonly used YIG oscillators for the majority of practical applications.

HISTORICALLY, HIGH-PERFORMANCE phase-lock-loop (PLL) frequency synthesizers have relied on yttrium-iron-garnet (YIG) oscillators featuring broadband operation and excellent phase noise.[1] YIG-tuned oscillators also offer very linear and repeatable tuning characteristics that simplify the synthesizer coarse tuning in multiloop schemes. These unique features provided the domination of the YIG-based designs in high-end applications such as test-and-measurement signal generators.

The disadvantages of YIG oscillators include high power consumption, large size, and relatively high cost. The main problem inherent to YIG technology, however, is its slow frequency tuning speed, owing to the high inductance of the tuning coil. The typical achievable switching time is in the milliseconds range; while many systems still work adequately with this tuning speed, many newer systems require frequency tuning speeds in the microsecond range together with the spectral purity of lower speed designs.[2] Predictably, this presents serious design difficulties and tradeoffs.

Voltage-controlled oscillators (VCOs) offer an alternative to YIG oscillators in a PLL synthesizer. They tune faster than YIG oscillators, typically in the microsecond range. In addition, the size, power consumption, and cost of VCOs are generally much lower compared to YIG devices. But the noise performance of a VCO is considerably worse than that of a YIG oscillator, which may restrict using a VCO in high-performance designs. Hence, it is a common belief (or perhaps a myth?) that VCO-based designs are not capable achieving low-phase-noise performance compared to their YIG counterparts.

Is there any way to improve VCO-induced noise to a degree where it may be used in lieu of a YIG oscillator? This can be answered by comparing the phase-noise behavior of two hypothetical oscillators (YIG and VCO) that utilize identical active device arrangements. The oscillator noise behavior is usually represented as

$$L \approx 10\log\left\{\frac{GFkT}{2P}\left[\left(\frac{f_0}{2Q}\right)^2\times\frac{f_c}{f^3}+\left(\frac{f_0}{2Q}\right)^2\times\frac{1}{f^2}+\frac{f_c}{f}+1\right]\right\}$$

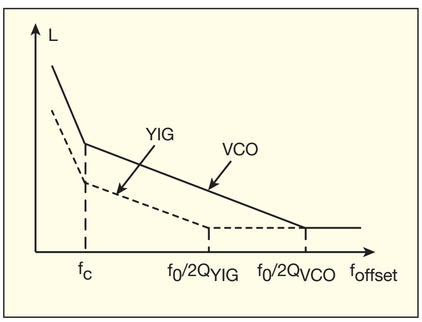
where

G = the active device gain,
F = the active device noise factor,
k = Boltzmann's constant,
T = absolute temperature,
P = the RF power applied to the resonator,
Q = the loaded quality factor of the resonator,
f0 = the oscillation frequency,
fc = the flicker-corner frequency of the active device, and
f = the offset frequency.

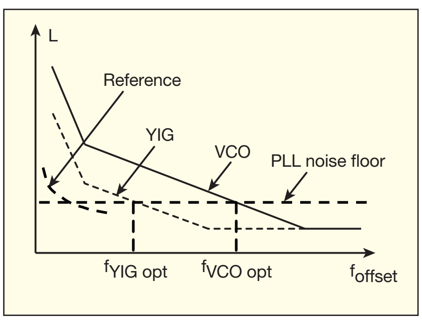
This expression is a well-known modification of Leeson's equation[3,4] that depicts oscillator phase-noise behavior in the offset frequency domain. Although the formula defines four basic frequency offset regions, in microwave oscillators the 1/f term is ignored because of the domination of 1/f^2 noise. This leads to the "classical" microwave oscillator phase-noise profile shown in **Fig. 1**.

At very high frequency offsets, both oscillators should demonstrate the same behavior (noise floor) defined by the ratio of the available RF power and thermal noise of the active device. The noise starts degrading at a rate of 20 dB per decade at lower frequency offsets from the carrier. The degradation start point is defined by the Q of the resonator used in the design. In the last region, where the flicker noise dominates, the phase noise increases at 30 dB per decade. Clearly, the VCO demonstrates significantly higher phase noise in comparison with the YIG-oscillator because of the difference in their resonator Q values.

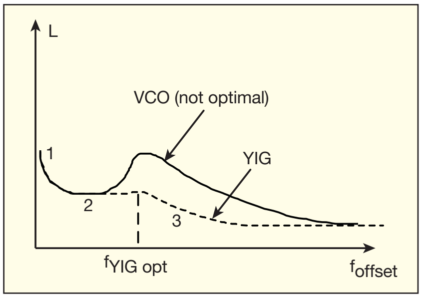
To evaluate the two sources in practical use, it is necessary to lock them to a low-noise reference source and compare the results. Those results depend on the available reference noise characteristics, PLL residual noise floor, and



1. These curves compare the phase-noise characteristics of free-running VCO and YIG oscillators.



2. Synthesizer phase noise depends not only on the VCO and YIG oscillators, but on the reference, PLL, and loop filter.



3. Using a loop bandwidth that is optimal for a YIG oscillator will not produce optimum performance when applied to a VCO over the same frequency range.

the loop-filter bandwidth as illustrated in Fig. 2 (with the all noise contributions recalculated to the synthesizer output frequency).

The loop filter bandwidth is preferably set to its optimal frequency—which is the cross point of the PLL multiplied noise and oscillator free-running noise curves—that provides the lowest overall phase noise response. A typical phase noise profile of a YIG-based synthesizer is shown in Fig. 3. The reference source noise normally dominates at very low frequency offsets (region 1), while a relatively flat noise plateau (region 2) occurs mainly because of the PLL residual noise limitations. Outside the loop filter bandwidth, the noise follows the free-running noise curve of the YIG oscillator (region 3).

Trying to lock the VCO within the same loop bandwidth will result in an inferior noise profile because of excessive VCO noise at these offsets. A smoother phase noise profile is obtained by locking the VCO within its own optimal bandwidth, as shown in Fig. 4. Since the VCO is now locked within a wider loop bandwidth, it locks much faster than the YIG oscillator. Nevertheless, the VCO phase-noise curve is still well above the YIG counterpart.

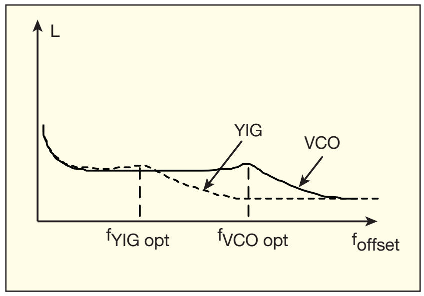
The difference in phase noise between the YIG- and VCO-based synthesizers is set by the PLL noise floor and free-running oscillator noise curves and is indicated as a hatched area in Fig. 5. Predictably, reducing the PLL noise floor and simultaneously widening the loop filter bandwidth-minimizes the difference, thus, making a VCO-based synthesizer behavior similar to its YIG counterpart.

Can a VCO-based design achieve performance comparable to that of a YIG-based frequency synthesizer? Assuming an ideal, noiseless PLL mechanism, the reference noise is translated at 20logN rate where N is PLL multiplication factor. Therefore, the output phase noise is still limited by the available reference that becomes a dominating factor. Modern commercial crystal oscillators provide phase-noise performance in the range of -160 to -180 dBc/Hz offset 10 kHz from a 100-MHz output frequency. These numbers can be potentially translated to -120 to -140 dBc/Hz at 10 GHz, which corresponds or even supersedes the performance of the best YIG oscillators at the same frequency settings.

In this example, YIG oscillator noise can be superior at higher frequency offsets (a few hundred kilohertz to a few megahertz), requiring a more complex reference scheme, as depicted in Fig. 6. The reference is a combination of a low-frequency oscillator (such as an OCXO) and high-frequency oscillator, such as a coaxial resonator oscillator (CRO) or dielectric resonator oscillator (DRO), locked to the OCXO. The loop bandwidth is chosen in such a manner that the phase noise at lower offsets is determined by the OCXO, while higher frequency offsets (from a few hundred kilohertz to a few megahertz) are covered by the free-running noise of the CRO or DRO.

Thus, the chain of two (or more) oscillators allows optimizing the phase-noise profile at any frequency offset and can be used in high-end synthesizer designs. In general, a high-Q, fixed-frequency, reference oscillator is capable of delivering a low-phase-noise signal comparable or better to that generated by a YIG oscillator at any frequency offset.

This design approach does not violate the laws of physics. In practice, the noise limitations are mainly set by PLL residual noise characteristics or, in other words, by a particular synthesizer architecture. The key principles in designing low-noise, fast-switching, VCO-based PLL synthesizers can be



4. Locking VCO and YIG oscillators within their own optimal loop bandwidths produces better results for both types of oscillators.

summarized by 1) using a low-noise reference source, 2) reducing the PLL residual noise floor, and 3) extending the loop filter bandwidth.

This concept has been practically implemented in QuickSyn™ frequency synthesizers manufactured by Phase Matrix (www.phasematrix.com). The product line includes models FSW-0010 and FSW-0020 with frequency ranges of 100 MHz to 10 GHz and 200 MHz to 20 GHz, respectively.

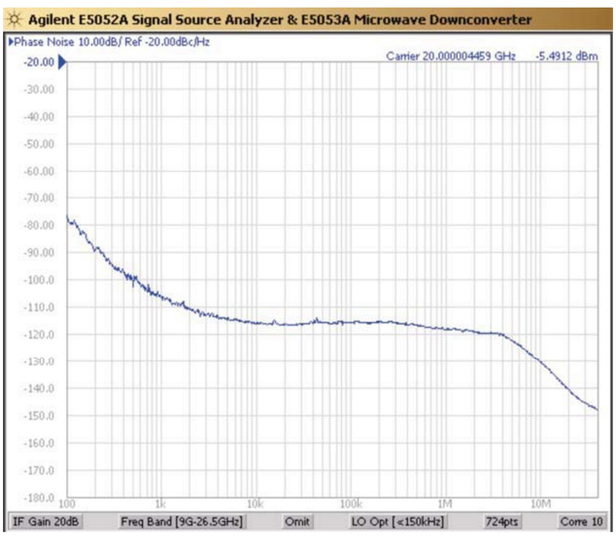
Both models employ a broadband VCO locked with a patented phase-refining technique. The technique offers almost "noiseless" frequency translation of utilized reference source (meaning that phase noise degradation is close to the "ideal" 20logN). This is achieved by replacing a frequency divider (normally used in PLL designs) with a frequency multiplier that reduces noise impact of a phase detector as well as other PLL components.[5]

The design incorporates a relatively inexpensive 100-MHz oven-controlled crystal oscillator (OCXO) reference oscillator that exhibits about -163 dBc/Hz noise floor starting from 10 kHz offset from the carrier. Thus, assuming the "ideal" frequency translation, it is reasonable to expect a -123 dBc/Hz phase-noise level at a 10-GHz output (40-dB degradation) or a -117 dBc/Hz phase-noise level at a 20-GHz output (another 6-dB degradation).

Figure 7 shows a phase-noise plot measured at 20 GHz with a model E5052A signal source analyzer and model E5053A downconverter from Agilent Technologies (www.agilent.com). It clearly shows that the measured noise is close to the predicted value. At lower output frequencies, phase noise is further improved at 6 dB per octave rate resulting from the employed frequency division scheme. For example, at a 5-GHz output and 10-kHz offset, the noise drops to about -128 dBc/Hz. These phase-noise characteristics allow using the VCO-based frequency synthesizer in many applications that typically required a YIG-based design because of its traditional advantages in close-to-the-carrier spectral purity. But in this frequency synthesizer scheme, the close-in phase noise of the VCO microwave source is improved by the frequency division scheme.

Furthermore, the plot reveals that the PLL bandwidth is close to 4 MHz that should result in extremely fast frequency settling. In reality, the switching speed is limited not only by the main loop dynamics but also by other synthesizer modules and digital control. The parameter is specified at 100 μs and is guaranteed for any frequency step within the entire operating range (i.e., from any frequency to any frequency). This switching speed is much faster than can be achieved with traditional YIG-based designs.

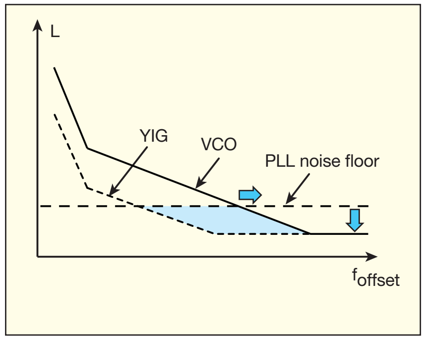
Another benefit of using a VCO in lieu of a YIG oscillator is reduced sensitivity to vibration (usually referred as "microphonics") as a result of the use of a low-mass VCO and very wide loop filter bandwidth. Although significant advances have been made in recent years in terms of smaller, cube-sized and even drop-in-packaged YIG oscillators, which were traditionally housed in large, cylindrical packages to accomodate the magnetic structure, a YIG oscillator for a given frequency tuning range is simply larger and with more mass than a VCO for that same frequency tuning range. For applications that are sensitive to the effects of vibration, such as in airborne avionics systems, the greater mass of the YIG oscillator translates into a greater potential for microphonically induced noise compared to a VCO, which is routinely packaged in a low-mass, surface-mount housing.



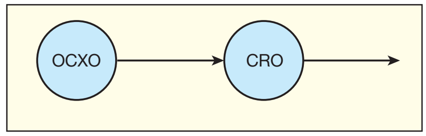
7. This phase-noise plot was measured at 20 GHz with a model E5052A signal source analyzer and model E5053A downconverter, both from Agilent Technologies (www.agilent.com).

At the frequency synthesizer design level, the small size of the free-running microwave oscillator leads to the reduced size occupied by the synthesizer core. This in turn leads to a small overall footprint for a system integrator and also allows implementing many other functions in a frequency synthesizer subsystem. These include output power leveling and control, blanking, frequency and power sweep functionality, list mode, and multiple analog and digital modulation options. In short, the QuickSyn™ synthesizer offers instrument-grade performance and functionality at a reduced, module-level size and cost.

VCO and YIG oscillators are key sources in PLL synthesizers. VCOs dominate in low-cost, low-to-moderate-performance designs. When high-performance, broadband, low-noise applications must be supported, the choice is more difficult. YIG-based solutions are usually simpler since the YIG oscillator can mask many design imperfections. One can easily achieve respectable phase noise performance with a fairly simple single- or dual-loop PLL by tolerating the slow tuning speed, large size, high power



5. Reducing the PLL noise floor and widening the loop filter bandwidth minimizes the difference in phase noise between YIG and VCO-based synthesizers.



6. A complex reference oscillator delivers optimal phase noise characteristics for carrier signals evaluated at any frequency offset.

consumption, and relatively high cost of a YIG oscillator.

Achieving the noise characteristics of a YIG-based synthesizer for a VCO-based design is not a trivial task. This calls for advanced solutions and also requires a great deal of effort to treat various "secondary" effects. Nevertheless, the need for faster tuning, smaller size, and lower cost makes the VCO an attractive alternative for the majority of practical scenarios. MWRF

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