An Innovative Approach in the Design of Fast-Switching Microwave Synthesizers

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***Abstract*—This paper presents a compact, broadband frequency synthesizer module, which covers 0.1 to 10 GHz frequency range with a 0.001 Hz step size. The synthesizer combines fast switching speed, low phase noise, and low spurious characteristics. The measured phase noise at an output frequency of 10 GHz and 10 kHz offset is –122 dBc/Hz. For an output frequency of 0.1 GHz and 10 kHz offset the phase noise is –150 dBc/Hz. Spurs do not exceed the –70 dBc level and the switching time of the main PLL is less than 10 uSec. This module can be used as a broadband, agile, high-fidelity signal source in a variety of test-and-measurement, communication, and surveillance systems.**

Keywords - frequency synthesizer; microwave source; signal generator; phase noise; switching speed

I. INTRODUCTION

The frequency synthesizer is a key element of virtually any microwave measurement setup. It generates a stimulus signal or is used as a local oscillator on the receiver side. Phase noise and spurious generated by the frequency synthesizer are critical parameters that impose the ultimate limit in the system's ability to resolve signals of small amplitude [1]. Another key parameter of the synthesizer that impacts overall system performance is the frequency switching speed [2-3]. The time spent by the synthesizer transitioning between frequencies becomes increasingly valuable since it cannot be used for data processing.

This requirement is illustrated with a 401-point sweep measurement (e.g., a network or spectrum analysis). Let's assume we are making a digital sweep measurement using a frequency source with 25 mSec switching speed (this is a typical number for traditional YIG-based bench-top signal generators). The measurement dead-time in this case exceeds 10 sec per sweep which may not be satisfactory in repetitive measurements (such as automated RF IC tests, etc.). The measurement throughput can be drastically improved with a faster source (e.g., 0.1 mSec) as indicated in Table 1.

TABLE I
MEASUREMENT DEAD-TIME COMPARISON

Source Switching Time	Number of Points	Dead-Time per Measurement
25 mSec	401	~10 Sec
0.1 mSec	401	~0.04 Sec

Thus, while many test-and-measurement systems still work adequately with millisecond switching speeds, newer requirements demand microsecond operation together with comparable spectral purity of the lower-speed designs.

II. ARCHITECTURE

Historically, high-performance microwave synthesizers have relied on YIG-tuned oscillators featuring broadband operation and excellent phase noise characteristics. However, the high power consumption, big size, and especially low tuning speed, inherent to YIG oscillators, have contributed to a shift to solid-state VCO architectures. VCO-based synthesizers are significantly faster; however, their phase noise has traditionally been considered to be inferior when compared to YIG-based designs.

We discuss an innovative direct-indirect architecture that provides a unique combination of fast-switching speed and very low phase noise characteristics. The phase noise within the loop filter bandwidth depends on the reference as well as residual noise characteristics of individual PLL components (such as phase detector, reference and feedback divider, loop filter, etc.) and is further degraded by large division ratios required to provide a high-frequency output with a fine resolution. In contrast to traditional approaches (which tend to minimize the PLL loop division ratio), the proposed design takes a more radical step by eliminating the divider from the PLL feedback path. Moreover, it inverts the PLL division ratio by applying a multiplication within the PLL as depicted in Fig. 1. This drastically improves both phase noise and spurious characteristics.

Furthermore, the PLL bandwidth is significantly extended in comparison to conventional PLL designs in order to suppress the VCO noise within the loop bandwidth. The optimum PLL bandwidth (which is the crosspoint of the PLL cumulative noise and VCO free-running noise) is found around 5 MHz. This results in extremely small frequency acquisition time and consequently fast switching speed. Additionally, the wide PLL bandwidth suppresses undesired microphonic effects.

A simplified block diagram of a frequency synthesizer developed with this concept is shown in Fig. 1. The main PLL includes a fundamental VCO covering the 5-to-10 GHz frequency range. The VCO is locked to a low-noise reference with the help of a frequency offset block generating course frequency steps. A desired frequency resolution of 0.001 Hz is

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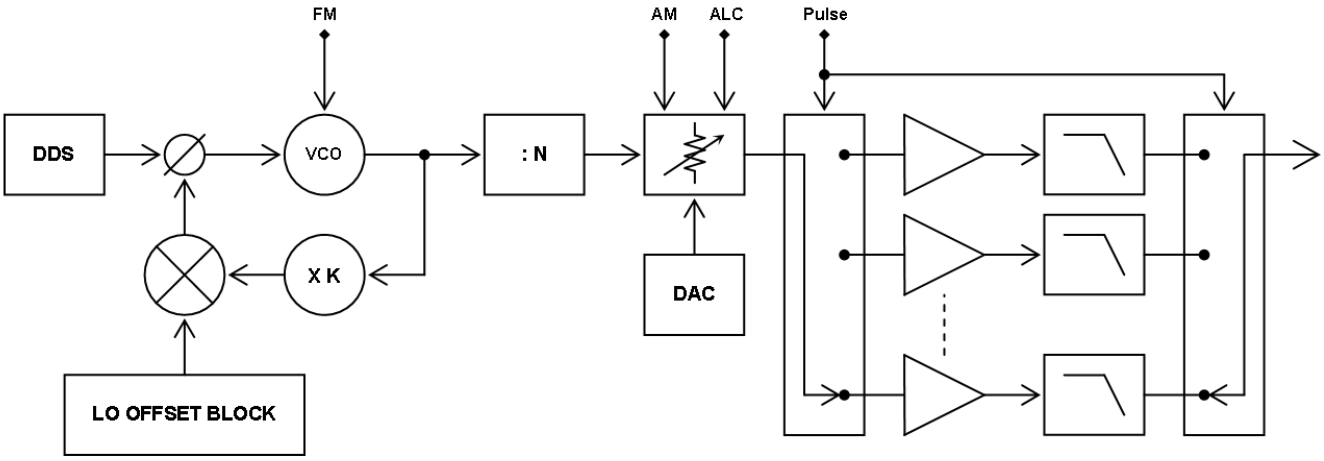

Figure 1. Simplified block diagram

provided with a DDS module that fills in the gaps between the LO offset steps. The DDS spurs are suppressed with a combination of hardware (upconversion followed by division) and software techniques discussed in [4].

The frequency coverage below 5 GHz is accomplished with a programmable frequency divider. The signal between 100 MHz and 10 GHz is amplified and filtered with a switched amplifier-filter bank that results in reduced harmonics. The signal level in front of the amplifiers is controlled with a variable gain attenuator. The attenuator is driven by a DAC that carries output power calibration functions as well. The attenuator can be also accessed directly to provide a closed-loop ALC capability. By adding an external coupler and RF detector, the signal from the detector can be fed back to the attenuator control input in order to close the loop. This configuration ensures precise, instrument-grade output power characteristics regardless of the output match.

The synthesizer includes a highly stable internal OCXO that sets the desired phase noise performance and also provides a 10-MHz reference signal to the outside world. The internal oscillator will automatically lock to an externally applied reference. The design also includes amplitude, frequency, and pulse modulator circuits shown simplistically in Fig. 1.

The synthesizer is built on a printed circuit board that is placed into a compact metal enclosure measuring 7 by 5 by 1 inches in dimensions (Fig. 2). The module can be controlled through SPI and USB interfaces, which are realized with a built-in processor. The processor supports all necessary frequency tuning algorithm calculations as well as a number of features such as output power calibration and control, independent frequency and power sweep, and list mode. All the

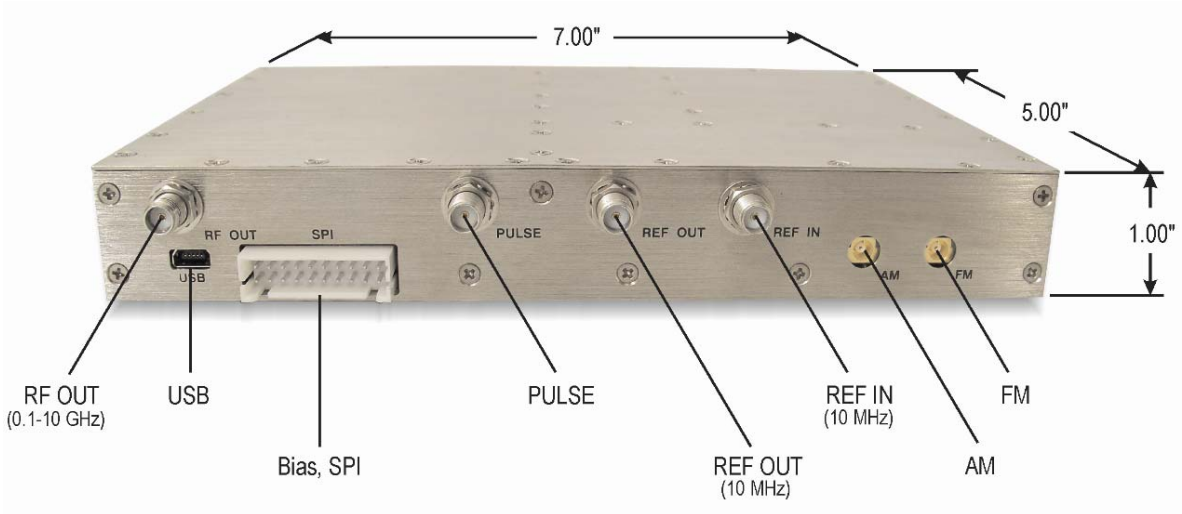

Figure 2. Frequency synthesizer module

signal and control connectors face the synthesizer front panel as illustrated in Fig. 2. The module is biased from a single +12V DC supply and includes custom-built active filters to prevent signal contamination. The overall power consumption does not exceed 20 Watts.

III. PERFORMANCE

The measurement results include output power, switching speed, phase noise, and spurious tests as indicated below.

A. Output Power

The maximum unleveled power is close to +20 dBm and can be calibrated between –25 and +15 dBm levels across the entire operating range. The power variations do not exceed ±1 dB as depicted in Fig. 3.

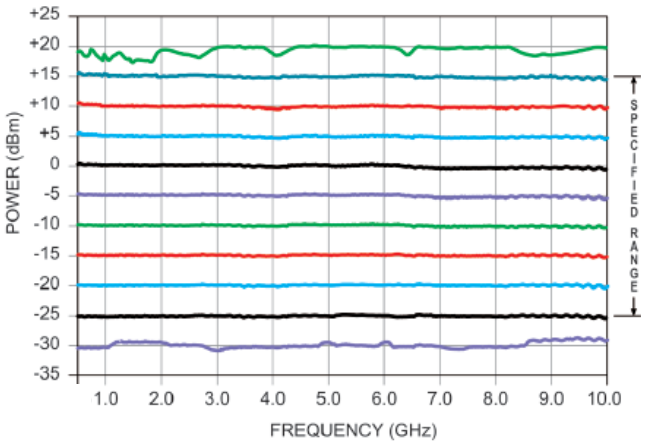

Figure 3. Output power response at various power settings

B. Switching Speed

The frequency switching speed of the main PLL loop is less than 10 uSec (to be within 1 MHz from the final frequency) and less than 20 uSec (within 50 kHz) as shown in Fig. 4.

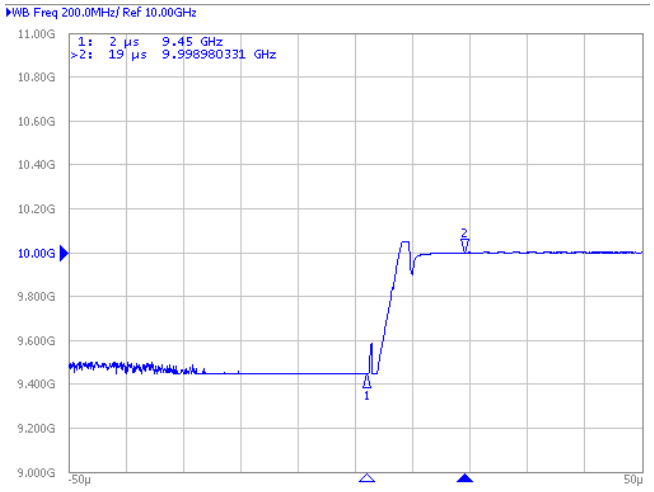

Figure 4. Switching speed measurement

However, the LO offset block as well as the synthesizer control add extra delays required to receive a tuning command, perform all necessary calculations, and program individual devices. The overall throughput time is in order of a few tens of microseconds and is specified at 100 microseconds.

C. Phase Noise

The phase noise plots taken at 10 GHz and 100 MHz outputs are shown in Fig. 5 and 6 respectively. The phase noise at 10 kHz offset is about -122 dBc/Hz with a 10 GHz output signal.

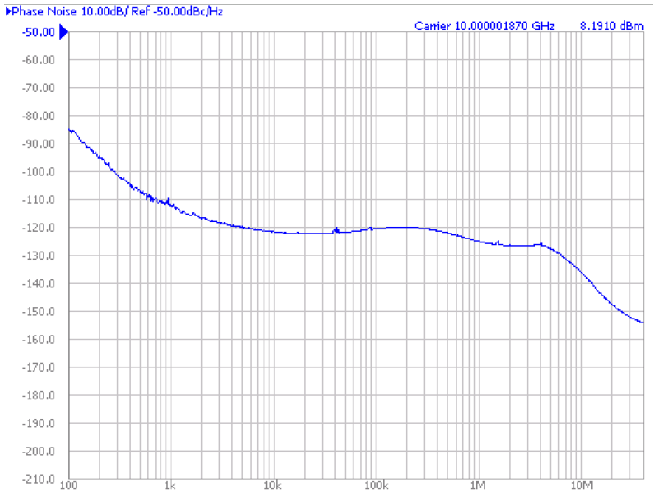

Figure 5. Phase noise at 10 GHz

The noise drops down to about -150 dBc/Hz at 100 MHz (limited by the divider and test setup noise floor). The phase noise profile also reveals that the loop bandwidth is roughly 5 MHz which results in fast tuning speed as mentioned above.

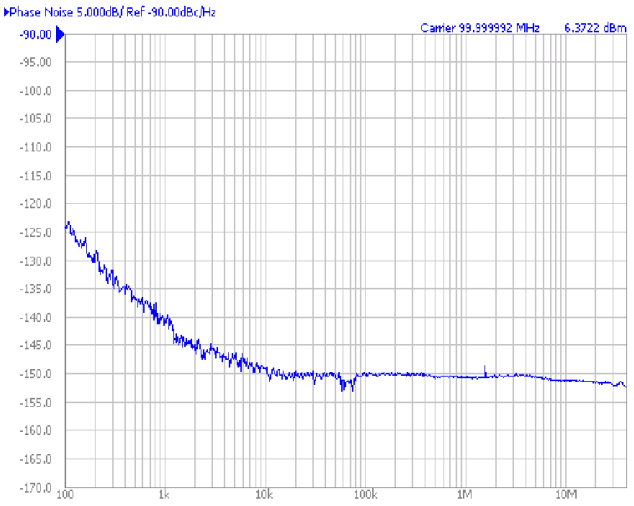

Figure 6. Phase noise at 100 MHz

D. *Spurious*

A 10 GHz spectrum plot is shown in Fig. 7; spurious levels do not exceed –70 dBc.

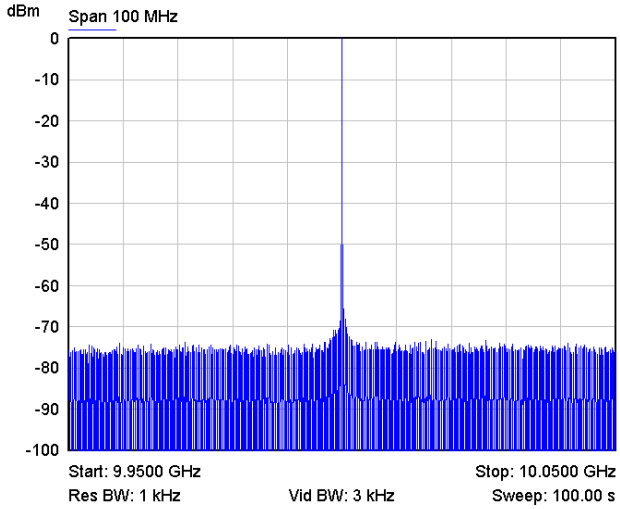

Figure 7. Output spectrum at 10 GHz

IV. CONCLUSIONS

A compact VCO-based frequency synthesizer has been developed. The measured characteristics are summarized in Table 2. The synthesizer covers the 0.1-to-10 GHz frequency range with a 0.001 Hz step size and 100 usec tuning speed that allows realizing digital sweep functions without sacrificing sweeping time. Furthermore, phase noise at 10 GHz is measured to be better than –120 dBc/Hz at 10 kHz offset. This corresponds to or even exceeds the phase noise performance of traditional YIG-based designs used in bench-top and rack-mountable instruments.

TABLE II
SYNTHESIZER CHARACTERISTICS

Parameter	Measurement
Frequency Range	0.1 – 10 GHz
Frequency Resolution	0.001 Hz
Switching Time	100 uSec
Output Power	-25 to +15 dBm
Phase Noise, 10 kHz offset	-122 dBc/Hz at 10 GHz -150 dBc/Hz at 0.1 GHz
Spurious	-70 dBc max.
Size	5 x 7 x 1 inches

These technical characteristics together with compact size will benefit various microwave measurement setups where a broadband operation, high spectral purity, and fast switching speed are simultaneously required. In addition to the test-and-measurement equipment, the developed frequency synthesizer can be used in many other applications including telecommunications and surveillance systems.

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