A Broadband, Low Phase Noise, Fast Switching PLL Frequency Synthesizer

Alexander Chenakin
Phase Matrix, Inc.
San Jose, CA
achenakin@phasematrix.com

***Abstract*—This paper presents a low phase noise, fast switching speed PLL synthesizer, which employs a simple and cost-effective direct-indirect architecture. The PLL residual noise floor of about -140 dBc/Hz is achieved by removing frequency division from the phase-locked loop, while the required frequency step is provided by multiplying and mixing the reference frequency. The measured phase noise at a 10 GHz output and 10 kHz offset is limited by the available reference at -120 dBc/Hz, while the tuning speed is less than 10 uSec.**

I. Introduction

The need for a low-cost, high-performance frequency synthesizer as a key component of virtually any test and measurement, communication, and monitoring system is recognized throughout the microwave community [1]. The industry feels persistent pressure to deliver higher performance, higher functionality, and lower cost synthesizer designs. However, the major technology challenge is in increasing the synthesizer tuning speed as dictated by the ongoing increase of the data rates of modern microwave systems [2]-[4]. The time spent by the synthesizer becomes increasingly valuable since it cannot be used for data processing.

This paper presents a fast switching speed PLL synthesizer, which employs an innovative direct-indirect architecture to achieve low phase noise characteristics. The PLL residual noise floor of about -140 dBc/Hz is achieved by removing frequency division from the phase-locked loop, while the required frequency step is provided by multiplying and mixing the reference frequency. This approach combines low-noise characteristics of direct analog schemes with a simplicity and low-cost benefits of PLL designs. The synthesizer concept and measurement results are discussed.

II. Synthesizer Concept

The direct analog synthesizer is today's most advanced technique offering unprecedented speed and phase noise performance [5], [6]. The desired signal is obtained by mixing reference frequencies followed by switched filters as depicted in Fig. 1. The key advantage of the indicated topology is extremely fast switching speed as well as the ability to generate very low phase noise output (limited by the noise of the available reference sources). The main disadvantages are limited frequency coverage and step size. Another serious problem is a large amount of undesired mixing products that have to be carefully planned and filtered out. Although a large variety of mixing and filtering organization schemes is possible, they tend to be hardware intensive if a small frequency step and wide frequency coverage are required. Therefore, while this approach offers

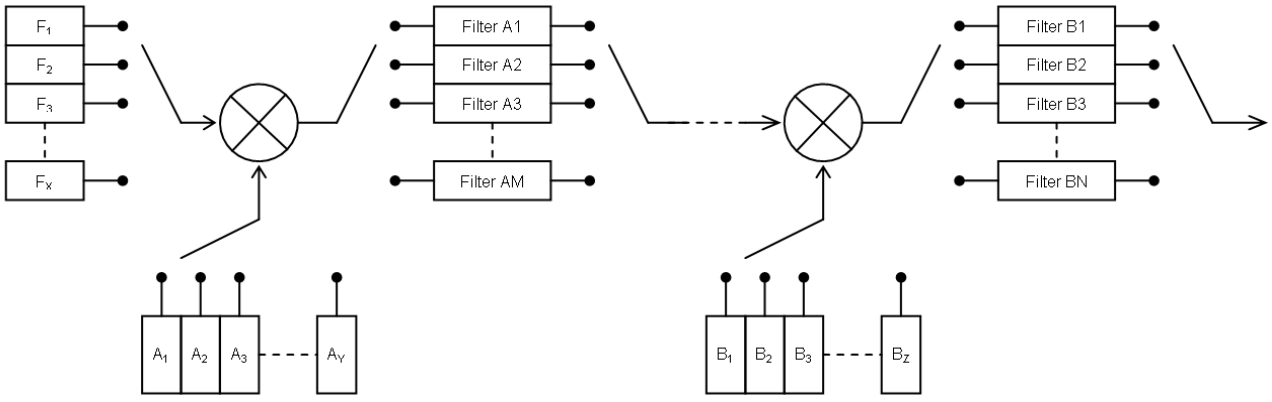

Figure 1. Direct Analog Synthesizer

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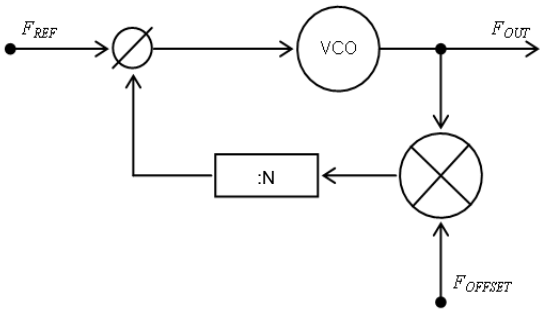

Figure 2. Frequency Offset

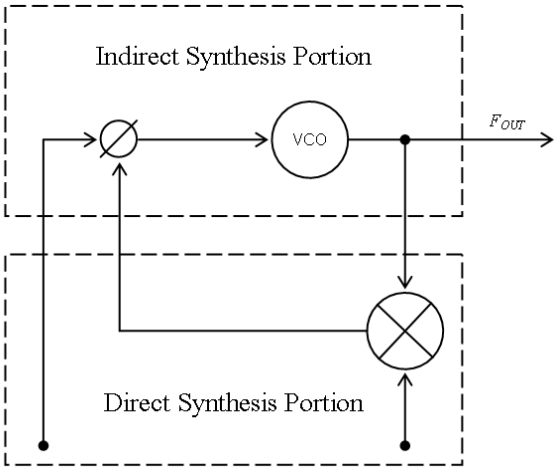

Figure 3. Synthesizer Concept

excellent tuning speed and phase noise characteristics, its usage is limited to applications where fairly high cost can be tolerated.

Indirect frequency synthesizers utilize phase-lock loop techniques offering much lower level of complexity in comparison with direct analog schemes [7]. The main disadvantages are longer frequency switching time (which is inversely proportional to the loop bandwidth and consequently step size) and considerably higher phase noise in comparison with direct analog techniques. The phase noise within the loop filter bandwidth depends on the reference as well as residual noise characteristics of individual synthesizer components (e.g., phase detector, reference and feedback divider, loop filter, etc.) and is further degraded by large division ratios required to provide a high-frequency output with a fine resolution.

The single-loop synthesizer's characteristics can be improved with a number of techniques such as fractional-N as well as employing a frequency offset (mixing) within the synthesizer feedback path as shown in Fig. 2. Since the frequency of the IF signal generated by the mixer is significantly smaller than the output frequency, required division coefficients are also smaller that result in improved phase noise performance. This technique works fairly well for narrowband applications; wide frequency bandwidths lead to higher IF that defeats the idea of this method.

This limitation is overcome in multiloop schemes by utilizing a variable offset frequency. Alternatively, the required IF frequency (for a given step size) can be obtained with a chain of mixers similar to the direct analog scheme shown in Fig. 1. In this case, the synthesizer combines both direct and indirect blocks as shown in Fig. 3. The direct analog portion acts as a mixer that generates an IF signal for the indirect (PLL) portion. The indirect portion provides a simple and effective mechanism to clean up undesired spurious signals generated by the direct portion.

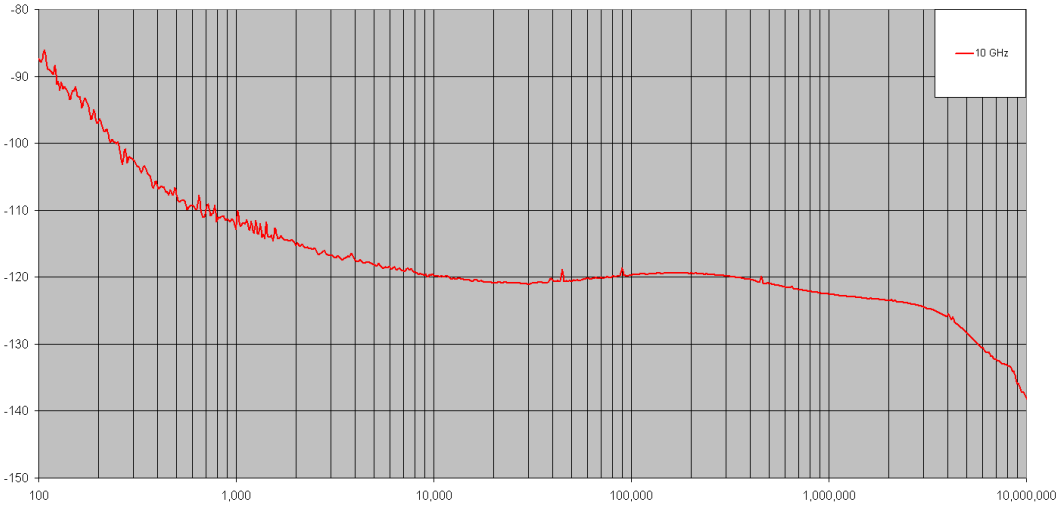

Figure 4. Phase Noise at 10 GHz

Thus, the main advantages of this approach are reduced levels of spurious signals owing to the low-pass filter action of the PLL and consequently much lower level of complexity compared to the traditional direct analog schemes. Another distinct advantage is reduced phase noise due to the absence of the divider in the PLL feedback path.

III. Experiment

In order to verify low phase noise capabilities of the utilized scheme, we run an experiment at a 10 GHz output using a simplified frequency offset configuration with the following parameters:

F_{OUT} = 10 GHz

F_{REF} = 50 MHz

N = 1

Loop BW = 3 MHz

Phase Margin = 75 degree

We utilized a custom-built 5-10 GHz fundamental VCO and Analog Device's ADF4002 phase detector IC with the phase noise floor better than -140 dBc/Hz at 50 MHz comparison frequency. All necessary offset signals were generated from a 100 MHz ovenized crystal oscillator, which exhibited about -163 dBc/Hz noise floor above 10 kHz. This phase noise can be potentially translated to -123 dBc/Hz at a 10 GHz output (assuming an ideal *20logN* degradation). Since the loop multiplication factor is reduced to 1, the output phase noise is expected to be mainly limited by the multiplied reference noise.

IV. Measurement Results

The measured phase noise performance at a 10 GHz output is shown in Fig. 4. The phase noise at 10 kHz offset is about -120 dBc/Hz that basically corresponds (within a few dB) to the multiplied noise of the utilized reference source. Some noise degradation is apparently due to the influence of other PLL components (e.g., loop filter, operational amplifier, bias, etc.). The phase noise at lower frequencies follows the *20logN* rule and was found about -126 dBc/Hz at a 5 GHz output and same frequency offset.

The phase noise profile also reveals that the loop bandwidth is about 3 MHz that results in fairly fast tuning speed performance. The switching speed was found to be less than 10 uSec and was limited by the utilized digital interface rather than the PLL itself. Spurious plots for 1 and 100 MHz frequency spans are presented in Fig. 5 and 6 respectively. The output signal looks clean and free of obvious perturbations down to -75 dBc level.

Desired frequency coverage between 3 and 9 GHz is obtained by splitting the VCO output into two sub-bands as depicted in Fig. 7. The upper branch utilizes a portion of the available bandwidth between 5 and 9 GHz that allows using a 9 GHz low-pass filter to suppress VCO harmonics above 10 GHz. The lower branch includes a divide-by-2 divider to bring the VCO output frequency down to 2.5 GHz. Similarly, the lower branch utilizes a portion of the available bandwidth between 3 and 5 GHz in order to achieve adequate harmonic suppression above 6 GHz. This approach provides 3 to 9 GHz overall frequency coverage with reduced harmonic content. The measured harmonics did no exceed -40 dBc across the entire band. Besides the improved harmonic performance, the utilized scheme allows optimizing synthesizer output power without the use of expensive broadband amplifiers. The output power was measured between +13 and +15 dBm.

V. Conclusions

A simple and cost-effective direct-indirect frequency synthesizer approach has been investigated. The approach combines low-noise characteristics of direct analog schemes with simplicity and low-cost benefits of conventional PLL

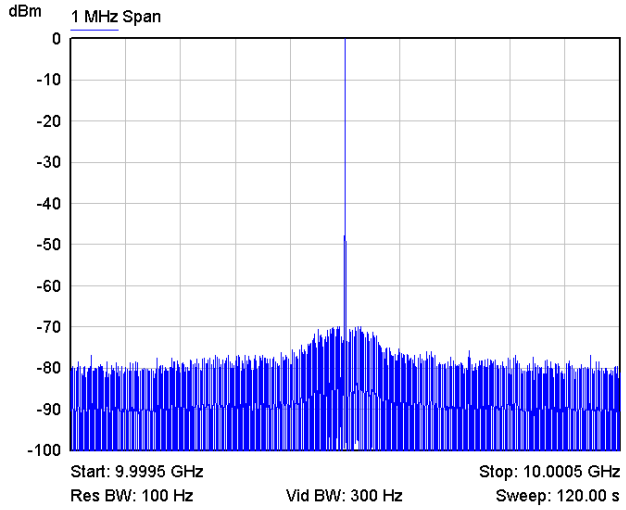

Figure 5. Spurious at 1 MHz Span

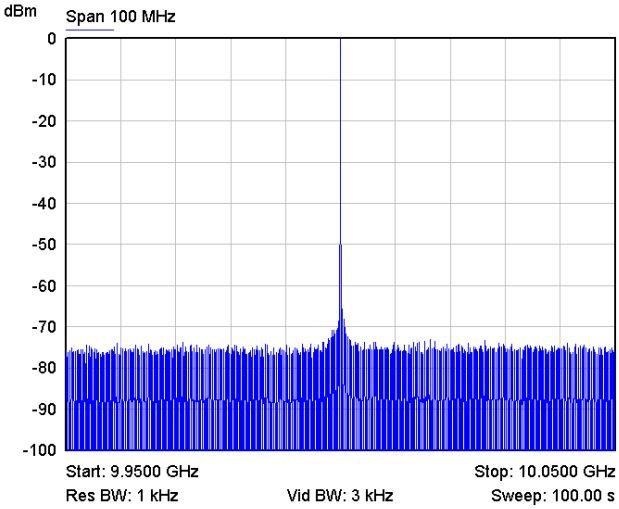

Figure 6. Spurious at 100 MHz Span

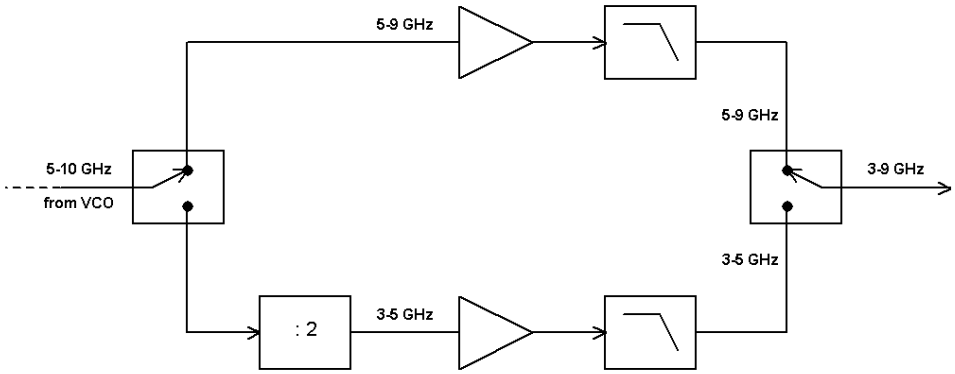

Figure 7. Synthesizer Output

designs. Using this approach, a 3-9 GHz low phase noise, fast switching speed frequency synthesizer prototype has been developed. The measured phase noise at a 10 GHz output and 10 kHz offset is -120 dBc/Hz, while the tuning speed is less than 10 uSec. The phase noise performance is mainly limited by the available reference and shows *20logN* improvement at lower output frequencies.

The measured spurious level does not exceed -75 dBc in respect to the main signal. The synthesizer output power is between +13 and +15 dBm across the band, while the harmonics do not exceed -40 dBc. Thus, the utilized architecture combines high-performance and low-cost characteristics and can be used in a variety of practical synthesizer designs.

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