A Small Form Factor 3-9 GHz Synthesizer Module for Use in Synthetic Instrumentation Applications

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novel 3-9 GHz fast frequency switching synthesizer module has been developed. The synthesizer employs a multi-loop VCObased design that delivers +15 to +19 dBm output power across the band. A built-in DDS provides sub-Hz frequency resolution with excellent spurious and phase noise characteristics. The developed module employs a "brick" form factor and can be used in a variety of synthetic instrumentation applications and platforms. The module's construction and measurement results are presented.

an emerging technology that offers a cost-effective modular approach for building complex test and measurement equipment. It enables the emulation of various traditional benchtop instruments employed in automatic test systems using a reconfigurable combination of core hardware and software components [1], [2].

The performance of synthetic instruments primarily depends on technical characteristics of their core modules. The need for a low-cost, highperformance frequency synthesizer as a key component of virtually any test and measurement system is recognized throughout the microwave community [3]-[5]. The indus-

Introduction

Synthetic instrumentation is

deliver higher performance, higher functionality, smaller size, lower power consumption, and lower-cost synthesizer designs. A key market demand is faster frequency tuning speed, as dictated by the ongoing increase of the data rates of modern microwave systems [6]. Addressing these needs, we introduce a novel, 3-9 GHz, VCO-based, fast-switching frequency synthesizer module compacted into a "brick" form factor (approximately 4" x 6" x 1.5"), which can be used in a variety of small form factor (VXI, PXI, LXI) synthetic instrumentation applications. The module's construction and measurement results are discussed below in the context of PXI as the target platform.

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Synthesizer Design

The module consists of two major parts: the microwave synthesizer and the reference block, as shown in Figure 1. The reference block is based on a 100 MHz highly stable ovenized crystal oscillator (OCXO) that serves as a reference for the microwave synthesizer. The reference block also includes a divide-by-10 divider to get a 10 MHz reference signal; both 10 MHz and 100 MHz outputs are provided on the front panel of the module. The internal OCXO can drive the module itself or can be automatically locked to an external 10 MHz reference if required. The module constantly monitors the presence of the external reference and frequency lock.

The microwave portion is based on a 5-10 GHz, fundamental, solid-state, voltagecontrolled oscillator (VCO) with an output that is split into two sub-bands, as depicted in Figure 2. The upper branch utilizes a portion of the available bandwidth (5 to 9 GHz) that allows the use of a 9 GHz

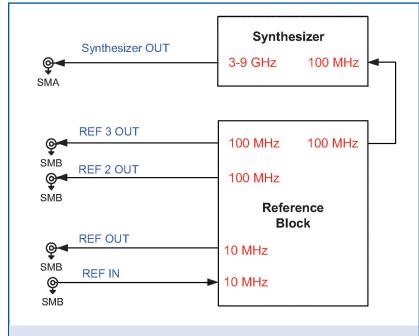


Figure 1: Module Block Diagram

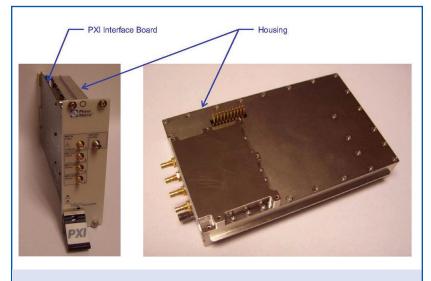


Figure 3: Prototype PXI Synthesizer Assembly

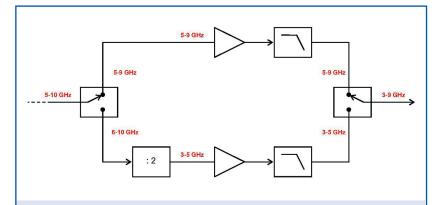


Figure 2: Block Diagram of the Synthesizer Output

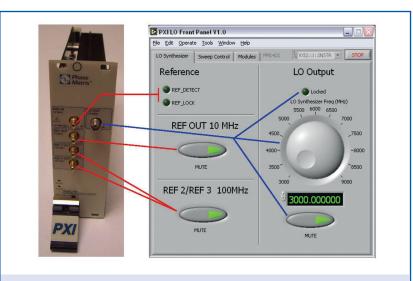
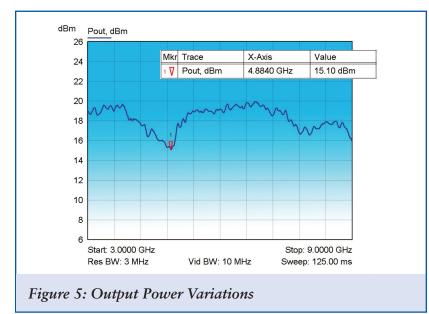


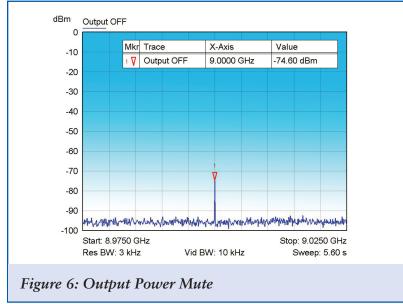
Figure 4: Synthesizer Control

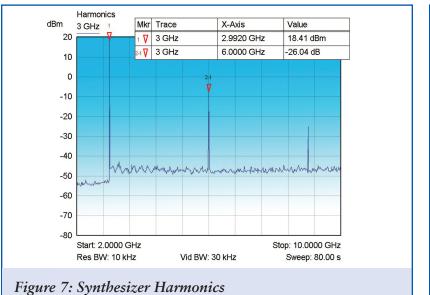
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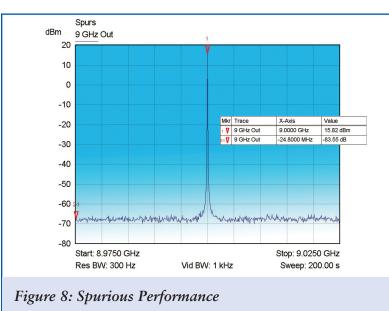
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and above. The lower branch includes a divide-by-2 divider 3 to 9 GHz overall frequency coverage with reduced harmonic content.

The VCO is locked to a built-in DDS device that provides sub-Hz frequency resolution without the common penalty of slower tuning and increased phase noise degradaels (in comparison with more a PXI chassis. copious PLL reference spurs), as discussed in more detail in Module Control

low-pass filter to suppress The VCO phase noise is effec- is hosted on a separate com- output can be muted to about relatively wide (a few hundred kHz) loop bandwidth as also GHz. This approach provides locking mechanism. A highfrequency and fairly low-noise OCXO is utilized along with phase noise performance.

> The synthesizer reference and dwell time. and microwave circuits are put into a metal housing (shown in Test Results Figure 3) to prevent interfer-

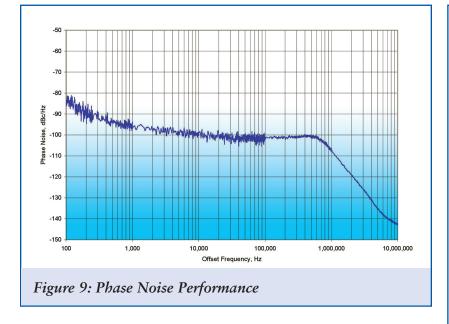
VCO harmonics from 10 GHz tively controlled by utilizing a puter. The GUI allows the -75 dBm level (worst case) user to set a desired output without disturbing the synthefrequency, monitor frequency sizer VCO (Figure 6). Since to bring the output frequency suggested in [6]. Thus, the lock, and mute the synthesizer the VCO remains locked, the down to 3 GHz. Similarly, the synthesizer phase noise with- output, as shown in Figure muting is inherently fast and, lower branch utilizes a portion in its PLL bandwidth mainly 4. On the reference side, the of the bandwidth $(3-\overline{5} \text{ GHz})$ depends on the multiplied ref- user can independently mute in order to achieve adequate erence noise as well as residu- 10 MHz and 100 MHz out- a uSec pulse width and on/off harmonic suppression above 6 al noise characteristics of the puts, monitor the presence of external 10 MHz signal, and check the reference lock. The software also allows sweepan advanced multi-loop archi- ing the synthesizer across the tecture to achieve desirable entire frequency range with programmable frequency step

The developed hardware protion. Since DDS-based designs ence from the outside environ- vides 3 to 9 GHz frequency are prone to increased spuri- ment and possible signal con- coverage with 0.1 Hz step ous content, both hardware tamination. A PXI interface size and less than 300 usec and software techniques are board is placed on top of the switching time. The maximum extensively utilized to suppress housing to deliver all bias volt- (unleveled) RF output power DDS spurs to negligible lev- ages and control signals from varies between +15 and +19 dBm, as shown in Figure 5. The output power variations are mainly due to the uti-[6]. Though PLL spurs domi- The module is controlled lized low-pass filters; this issue nate, they are easily managed through a standard PXI bus will be addressed in the next by optimizing the loop filter. with a LabView GUI, which design iteration. The signal erence noise (as well as resid-

therefore, can be potentially used for pulse modulation with ratio greater than 80 dB.

The synthesizer's output spectrum purity is depicted in the next few plots. The harmonics do not exceed the -25 dBc level across the entire band; the worst case at 3 GHz is shown in Figure 7. A typical spurious plot is presented in Figure 8; the spectrum looks clean and free of obvious perturbations down to the -80 dBc level. This demonstrates the effectiveness of the employed DDS spur suppression algorithm and careful loop filter design.

The synthesizer's phase noise plot taken at 3 GHz is presented in Figure 9. The noise at low frequency offsets depends on the multiplied ref-



set-up, which brought its own contribution to the indicated plot). The noise between 10 and 100 kHz is mainly attributable to the PLL components; References above 1 MHz, the VCO's free-running noise dominates. The module exhibits about -100 dBc/Hz phase noise at 10 and 100 kHz offsets at a 3 GHz output. Noise perfor- Instruments: A New Horizon," mance at higher frequencies Microwave Journal, March degrades slightly due to the 2006, pp. 22-36. employed frequency plan. The noise plot also reveals the loop Synthesizers bandwidth of a few hundred kHz that results in fast tuning Microwaves & RF, March speed, as mentioned above.

The unit delivers 0 dBm reference signals at 10 and 100 MHz, which can be independently muted if required. It also accepts an external 10 MHz reference between -15 and +15 dBm to align the internal reference, as shown in Figure 10. The synthesizer & Sons, 1987. module power consumption does not exceed 15 Watts.

Conclusions

A small form factor, highly integrated, fast switching speed frequency synthesizer module has been developed. The synthesizer employs a multi-loop VCO-based design that delivers +15 to +19 dBm power between 3 and 9 GHz. opment of advanced frequency A built-in DDS, powered by a sophisticated spur suppression algorithm, provides fine Chenakin can be reached by frequency resolution of 0.1 Hz with excellent spurious e-mail at achenakin@phasemaand phase noise characteris- trix.com. The company webtics. The module also delivers site is www.phasematrix.com. highly stable 10 and 100 MHz reference signals, which can BS and MS degrees in electribe automatically locked to an *cal engineering with a special*external 10 MHz reference if *ization in RF and Microwaves* required. The module features from UC Davis in 1993 and low power consumption and 1995, respectively. He has

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ual noise of the measurement can be used in a variety of synthetic instrumentation applications and platforms, including PXI, VXI, and LXI.

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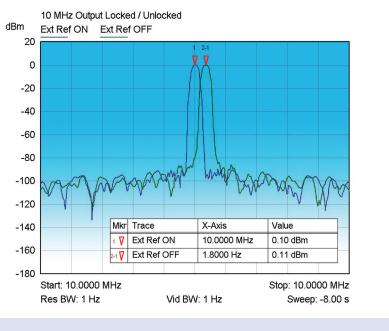


Figure 10: Reference Lock

previously designed cellular base station power amplifiers 1. M. Granieri, "Synthetic and signal sources for Agilent Technologies and Gigatronics. Presently he is an RF and Microwave Design Engineer in the Frequency Synthesis Group at Phase Matrix, Inc. Mr. Ojha can be reached at 408-954-6433 and sojha@phasematrix.com.

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