Phase Noise Suppression in PLL Synthesizers

Alexander Chenakin, Suresh Ojha, Nikolay Shtin

[Summary] The RF/microwave industry feels persistent pressure to deliver higher performance frequency synthesizer designs. Phase noise is a critical parameter that imposes the ultimate limit in the system's ability to resolve signals of small amplitude. Today's systems demand low phase noise per-formance without compromising other characteristics such as frequency coverage, resolution and spurious. This article reports a new methode for residiual phase noise suppression using frequency multiplication within phase lock loop. This method was successfully used in the Rubidium™ frequency synthesizers product line. Phase noise of −140 dBc/Hz at 10 GHz output and 10 kHz offset was reported.

1 Introduction

Microwave signal generators are among the most challenging of high-frequency designs. Overall, the industry feels persistent pressure to deliver higher-performance synthesizer designs[1]. Phase noise is a critical parameter that imposes the ultimate limit in the system's ability to resolve signals of small amplitude. Today's systems demand low phase noise performance without compromising other characteristics such as frequency coverage, resolution and spurious. This article reports a new method for residual phase noise suppression using frequency multiplication within phase lock loop (PLL).

2 PLL Phase Noise Behavior

Synthesizer characteristics depend heavily on a particular architecture. Indirect PLL synthesizers (Figure 1) use a voltage-controlled oscillator (VCO) to generate an output signal at microwave frequencies that is in a certain relationship with the reference signal[2-10].

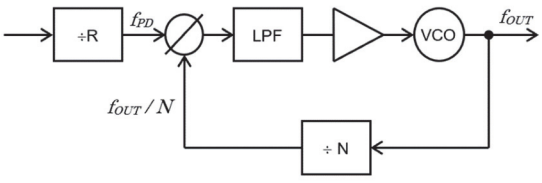

Figure 1 Single loop PLL synthesizer

This signal is fed back to a phase detector through a frequency divider with a variable frequency division ratio N. The other input of the phase detector is a reference signal equal to a desirable step size. The phase detector compares the signals at both inputs and generates an error voltage that, following filtering and optional amplification, slews the VCO until it acquires the lock frequency given by

$$f_{OUT} = f_{PD} / N$$

where f_{PD} is the comparison frequency at the phase detector inputs. The frequency tuning is achieved in discrete frequency steps equal to f_{PD} by changing the division coefficient N.

The major advantages of PLL synthesizers are reduced levels of spurious signals owing to the low-pass filter action of the loop, and much lower level of complexity compared with the direct analog synthesizers. The main disadvantage is considerably higher phase noise in comparison with direct analog schemes. The phase noise within the loop filter bandwidth is given by:

$$L_{PLL} = L_{\Sigma PD} + 20 \log N$$

where $L_{\Sigma PD}$ is phase noise of the reference signal, reference and feedback dividers, phase detector, LPF, and loop amplifier recalculated to the phase detector input. In other words, the phase noise generated by PLL components is degraded by large division ratios required to provide a high-frequency output with a fine resolution. For example, in order to get 10 GHz output with 1 MHz step size, the feedback divider ratio has to be 10000, which corresponds to 80 dB phase noise degradation. Thus, the conventional single-loop architecture suffers from poor phase noise performance. It is usually utilized in non-demanding applications or when low cost is the major concern.

The PLL synthesizer's main characteristics can be drastically improved using frequency conversion (mixing) within the synthesizer feedback path as shown in Figure 2. The idea is to convert the VCO output to a much lower frequency with the aid of a mixer and an offset frequency source. In certain

scenarios (e.g., when the operating frequency range is narrow) it is possible to eliminate the feedback frequency divider completely. In this case, the loop division coefficient equals one and no phase noise degradation occurs.

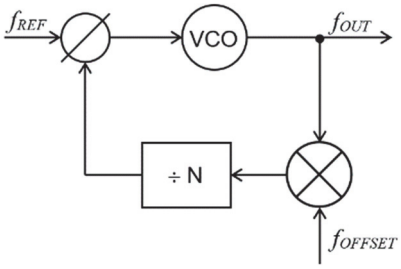

Figure 2 Frequency mixing within PLL feedback path

Moreover, one can further reduce PLL components residual noise by inserting a frequency multiplier into the feedback path instead of a divider as depicted in Figure 3.

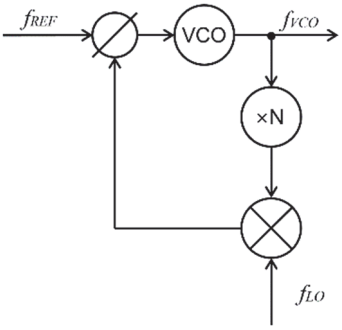

Figure 3 Frequency multiplication within phase-lock loop

In this case, the frequency multiplier acts exactly opposite to a frequency divider, i.e. it does not degrade but rather suppresses residual phase noise at the same 20log$N$ rate. Thus, there can be three basic scenarios constructing a PLL as follows:

N>1 – a frequency divider within PLL loop (residual phase noise is degraded at 20log$N$),

N=1 – no division within PLL loop (residual phase noise is not degraded),

N<1 – a frequency multiplier within PLL loop (residual phase noise is improved at 20log$N$).

3 Practical Implementation

This approach was successfully used in the Rubidium™ signal generators recently introduced by Anritsu Company[11]. The synthesizer core is based on a proprietary 2-20 GHz YIG oscillator that is locked to an internal reference extracted and distributed by direct analog means as illustrated in Figure 4.

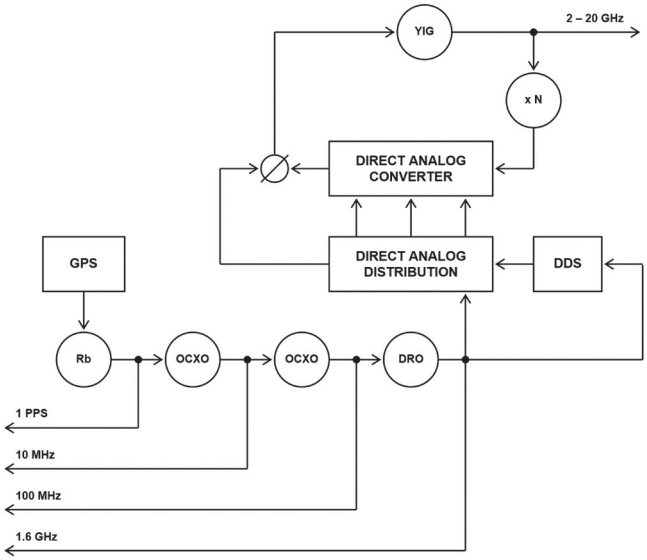

Figure 4 Practical implementation

The analog downconverter is essentially a chain of mixers, no divider is utilized. The YIG output signal is downconverted by the direct analog converter that eliminates any frequency divider and, therefore, phase noise degradation within the phase lock loop. Furthermore, a switched frequency multiplier (Figure 5) is inserted into the loop that provides additional residual PLL noise suppression[12].

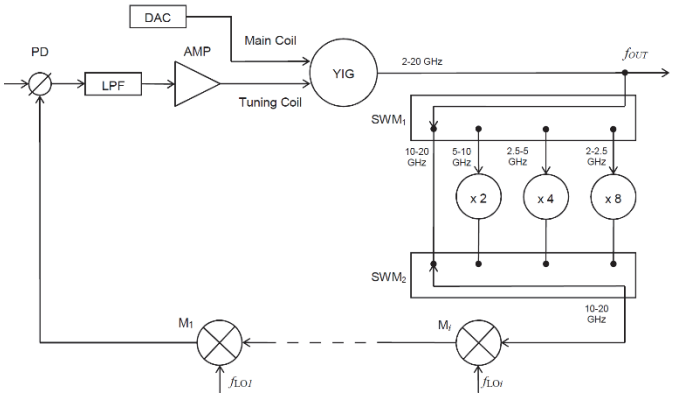

Figure 5 Switched frequency multiplier details

As a result, the presented architecture provides essentially noiseless PLL mechanism, meaning it translates synthesizer's reference noise with minimal added phase noise degradation. Note that the synthesizer phase noise is still limited by phase noise of available reference source. In our case, a three-component combined reference is utilized to provide the lowest possible phase noise at any given frequency offset. We utilize a chain that consists of a 10 MHz OCXO, 100 MHz OCXO and 1.6 GHz DRO. The DRO is custom-built design shown in Figure 6. Its phase noise

measured at 1.6 GHz output and 10 kHz offset was about −158 dBc/Hz. Furthermore, the combined reference is disciplined by a rubidium atomic clock that introduces a much higher degree of stability compared to a conventional OCXO-based reference.

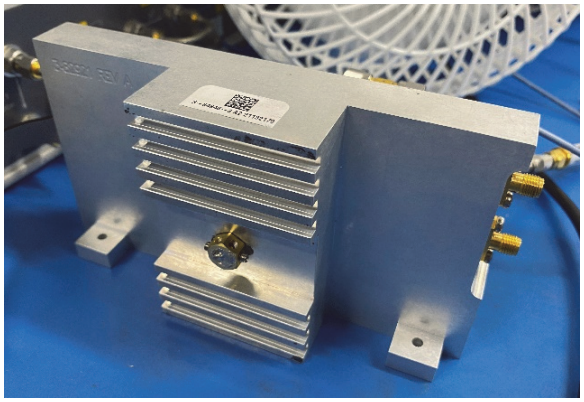

Figure 6 Custom-built 1.6 GHz DRO

4 Test Results

This concept was used in the development of Rubidium™ frequency synthesizers shown in Figure 7. The synthesizer covers 9 kHz to 20 and 43.5 GHz with 0.001 Hz resolution and excellent spectral purity. The measured phase noise at 10 GHz output is shown in Figure 8. Phase noise of −140/dBc was measured at 10 kHz offset that is better than traditional signal generators currently available on the market. Furthermore, it follows the fundamental 20log$N$ rule based on its DRO reference. This proves the "noiseless" concept used in the development of this synthesizer. Phase noise at our frequencies from 2 to 20 GHz followed the 20log$N$ rule due to the "noiseless" architecture (i.e. phase noise at 5 GHz output was 6 dB better within PLL bandwidth and so on).

Figure 7 Rubidium™ frequency synthesizer

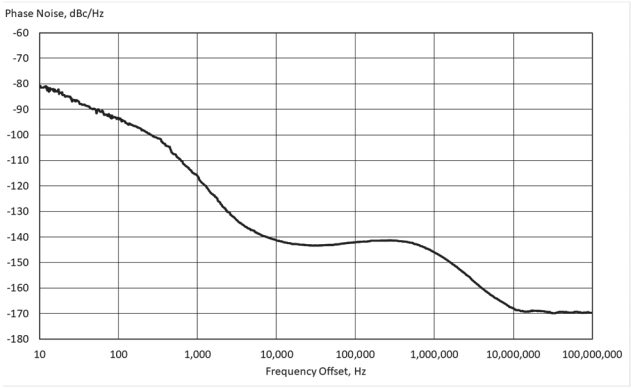

Figure 8 Phase noise at 10 GHz

5 Conclusions

This article reports a new method for residual phase noise suppression using frequency multiplication within PLL loop. The multiplier works exactly opposite to a frequency divider, thus, suppressing phase noise at 20log$N$ rate. This method was successfully used in the Rubidium™ frequency synthesizers product line. Phase noise of −140 dBc/Hz at 10 GHz output and 10 kHz offset was achieved using a combined reference source. Further improvements are possible using better reference sources such as sapphire-loaded cavity oscillators or optoelectronics methods.

References

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Author

Alexander Chenakin
Service Infrastructure Solutions
US Division
Test & Measurement Company

Suresh Ojha
Service Infrastructure Solutions
US Division
Test & Measurement Company

Nikolay Shtin
Service Infrastructure Solutions
US Division
Test & Measurement Company